NTE7483
Integrated Circuit
TTL – 4–Bit Binary Full Adder with Fast Carry

Description:

The NTE7483 is a 4–bit binary full adder in a 16–Lead plastic DIP type package that performs the addition of two 4–bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This device features full internal look–ahead across all four bits generating the carry term in ten nanoseconds (typ). This capability provides the system designer with partial look–ahead performance at the economy and reduced package count of a ripply–carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Features:

- Full–Carry Look–Ahead Across the Four Bits
- Systems Achieve Partial Look–Ahead Performance with the Economy of Ripple–Carry
- The NTE74283 is Recommended for New Design as it Features Supply Voltage and GND on Corner Pins to Simplify Board Layout.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage, V_{IN} 5.5V
Interemitter Voltage (Note 2) 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.
Note 2. This is the voltage between two emitters of a multiple–emitter transistor. This rating applies between the following pairs: A1 and B1, A and B2, A3 and B3, A4 and B4.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current Any Output Except C4	I_{OH}	–	–	–800	μA
Output C4		–	–	–400	μA
Low–Level Output Current Any Output Except C4	I_{OL}	–	–	16	mA
Output C4		–	–	8	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = –12mA	–	–	–1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 4mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	–1.6	mA
Short–Circuit Output Current Any Output Except C4	I_{OS}	V_{CC} = MAX, Note 5	–18	–	–55	mA
Output C4			–18	–	–70	mA
Supply Current All B Low, Other Inputs at 4.5V	I_{CC}	V_{CC} = MAX, Outputs Open	–	56	–	mA
All Inputs at 4.5V			–	66	110	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 5. Not more than one output should be shorted at a time.

Switching Characteristics: (V_{CC} = 5V, R_L = 667Ω, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From C0 Input to Any Σ Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF	–	14	21	ns
	t_{PHL}		–	12	21	ns
Propagation Delay Time (From A_i or B_i Input to Σ_i Output)	t_{PLH}		–	16	24	ns
	t_{PHL}		–	16	24	ns
Output Enable Time (From C0 Input to C4 Output)	t_{PZH}	R_L = 780Ω, C_L = 15pF	–	9	14	ns
	t_{PZL}		–	11	16	ns
Propagation Delay Time (From A_i or B_i Input to C4 Output)	t_{PLH}		–	9	14	ns
	t_{PHL}		–	11	16	ns

Function Table:

Input				Output					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH Level

L = LOW Level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Pin Connection Diagram