

74LS364 Flip-Flop

Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 8-bit positive edge-triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-State Output Enable control
- Independent register and 3-State buffer operation

DESCRIPTION

The '364 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition,

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS364	50MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS364N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

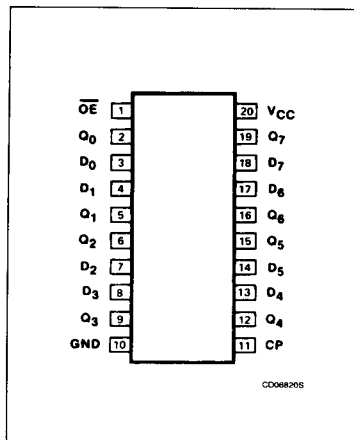
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

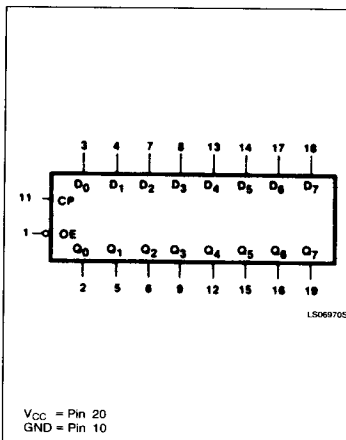
tion, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to

help minimize problems that signal and ground noise can cause on the clocking operation.

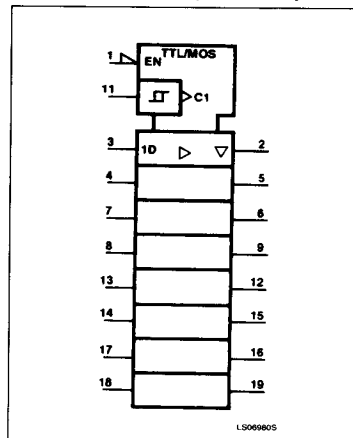
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

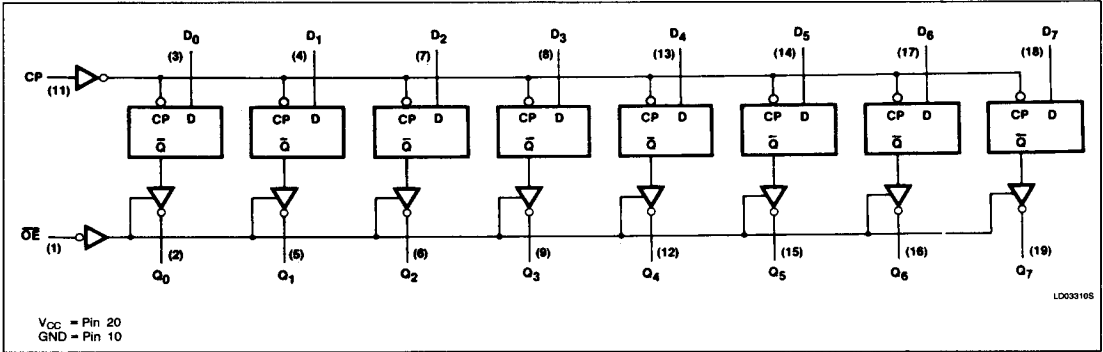


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The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-State buffer by driving the output about 1V closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		$Q_0 - Q_7$
Load and read register	L	\uparrow	l	L	L
	L	\uparrow	h	H	H
Latch register and disable outputs	H	\uparrow	l	L	(Z)
	H	\uparrow	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
 \uparrow = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

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RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IH}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-2.6	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74LS364			UNIT
			Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	3.65			V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$		0.35	0.5	V
		$V_{IL} = \text{MAX}, I_{OL} = 12\text{mA (74LS)}$		0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_O = 3.65\text{V}$			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_O = 0.4\text{V}$			-20	μA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			0.1	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-0.4	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-30		-130	mA
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}, \overline{OE} = 4.5\text{V}$		42	70	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74LS		UNIT
			$C_L = 45\text{pF}$, $R_L = 667\Omega$		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		33 34	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28	ns
t_{PZL}	Enable time to LOW level	Waveform 3		36	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5\text{pF}$		18	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5\text{pF}$		24	ns

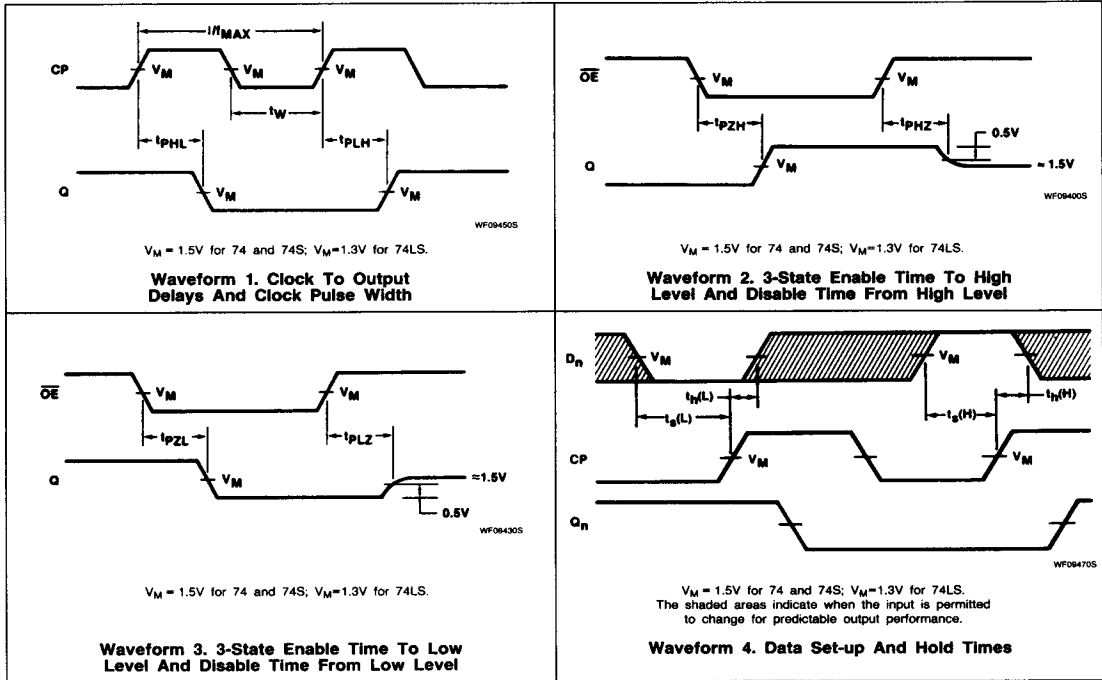
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W	Clock pulse width	Waveform 1		ns
t_s	Set-up time, data to clock	Waveform 4		ns
t_h	Hold time, data to clock	Waveform 4		ns

AC WAVEFORMS



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TEST CIRCUITS AND WAVEFORMS

