Signetics

74LS765
DRAM Controller

DRAM Dual-Ported Controller
Preliminary Specification

Logic Products

FEATURES

- **Allows two microprocessors to access the same bank of DRAM**
- **Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation**
- **9 address output pins allow control of up to 256K DRAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **Same as LS764 but without input latch**
- **30MHz Maximum Clock rate**

DESCRIPTION

The 74LS765 DRAM Dual-Ported Controller is a high speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'LS765 unlatched option eliminates the address input latch to facilitate use with latched address outputs.

The device is available in a 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS765	45ns	215mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS765N*
PLCC-44	N74LS765A**

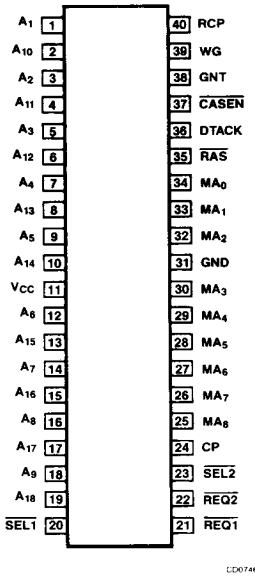
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

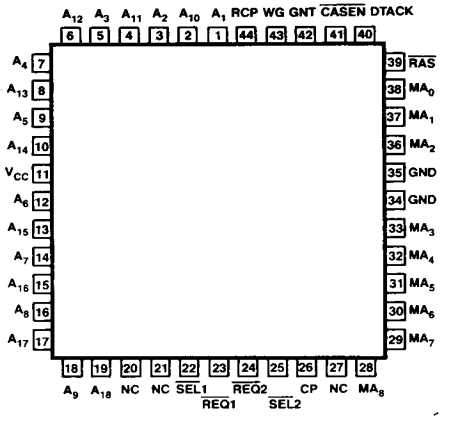
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$\overline{REQ}_1$, $\overline{REQ}_2$	Request inputs (active LOW)	1LSUL
CP	Clock input	1LSUL
RCP	Refresh clock input	1LSUL
A1 – A18	Address inputs	1LSUL
GNT	Grant output	60LSUL
$\overline{SEL}_1$, $\overline{SEL}_2$	Select outputs (active LOW)	60LSUL
DTACK	Data transfer acknowledge output	60LSUL
$\overline{RAS}$	Row address strobe (output active LOW)	60LSUL
WG	Write gate output	60LSUL
$\overline{CASEN}$	Column address strobe enable output (active LOW)	
MA0 – MA8	Address outputs	60LSUL

NOTE:
One 74LS Unit Load (LSUL) is defined as: 20μA in the HIGH state and 0.4mA in the LOW state.

PIN CONFIGURATION





BLOCK DIAGRAM