Silicon NPN Power Transistors 2SD1739

DESCRIPTION

·With TO-3PFa package
·Wide area of safe operation
·High voltage,high speed

APPLICATIONS

·Horizontal deflection output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

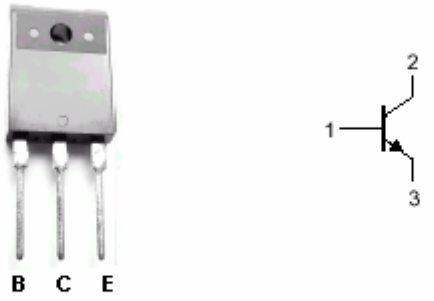

Fig.1 simplified outline (TO-3PFa) and symbol

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	700	V
V_{EBO}	Emitter-base voltage	Open collector	7	V
I_C	Collector current		6	A
I_{CM}	Collector current-peak		18	A
I_B	Base current		2.5	A
P_C	Collector power dissipation	T_C=25□	100	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CEsat}	Collector-emitter saturation voltage	I_C=5A ;I_B=1.2A			8.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=5A ;I_B=1.2A			1.5	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=1mA ;I_C=0	7			V
I_{CBO}	Collector cut-off current	V_{CB}=750V; I_E=0			10	μA
		V_{CB}=1500V; I_E=0			1	mA
I_{EBO}	Emitter cut-off current	V_{EB}=5V; I_C=0			10	μA
h_{FE}	DC current gain	I_C=1A ; V_{CE}=5V	6		30	
f_T	Transition frequency	I_C=1A ; V_{CE}=10V		2		MHz

Switching times

t_{stg}	Storage time	I_C=5A; I_{B1}=1A I_{B2}=-2A; V_{CC}=200V		1.5		μs
t_f	Fall time			0.2		μs

PACKAGE OUTLINE

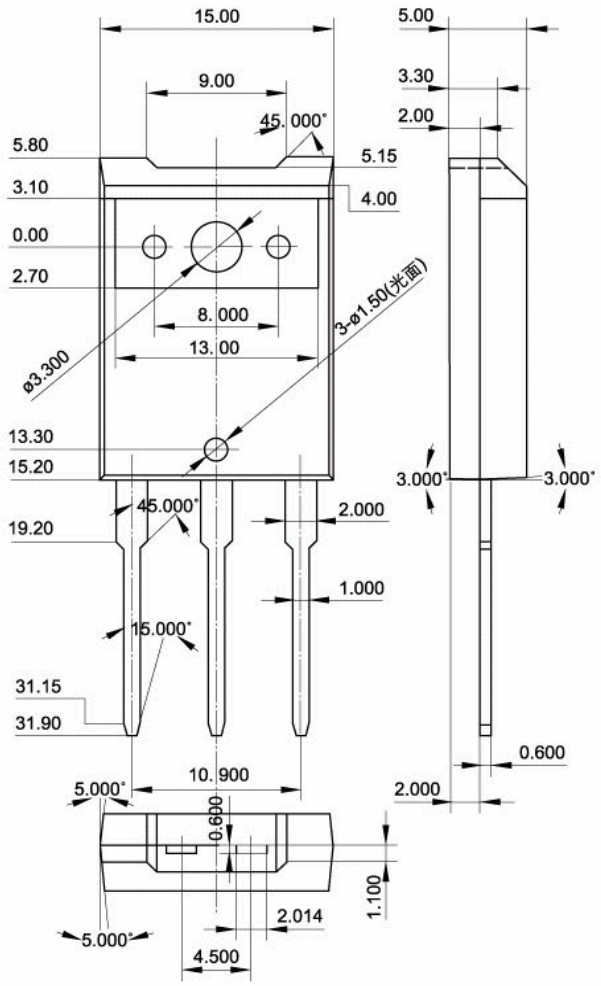

Fig.2 Outline dimensions (unindicated tolerance:±0.30mm)