Zerynth®

ZM1 Datasheet

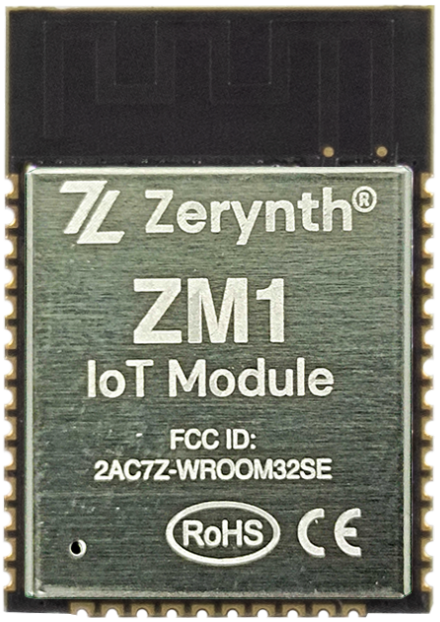


Table of Contents

Introduction

This datasheet provides information on how to use the ZM1 module in your application.

The ZM1 is part of the Zerynth hardware family that provides products with various features, different memory sizes, packages and peripherals.

Related documents and links:
Zerynth Documentation (docs.zerynth.com).

Overview

The Zerynth Module ZM1 is a dedicated customized version of the **ESP32-WROOM-32SE** Module. The Module is certified RoHS, CE/RED, e FCC (EU e US).

The ZM1 Module mounts onboard the ESP32-D0WD microcontroller, and is designed to be scalable and adaptive. The CPU clock frequency is adjustable from **80 MHz to 240 MHz**, With an embedded **16 MB** of SPI Flash memory and integrates a rich set of peripherals, ranging from Hall sensors, Capacitive touch sensor, SD interface, Ethernet, High speed SPI, UART, I2S e I2C.

Inside the ZM1, **the crypto element ATECC608A** from Microchip has been integrated to handle secure connections in an easy manner, exchanging certificates and keys, encrypting messages over TLS protocol and using secure authentication procedures.

Qualifications and Approvals

Please refer to the full certifications at the espressif certification page.

Key Features

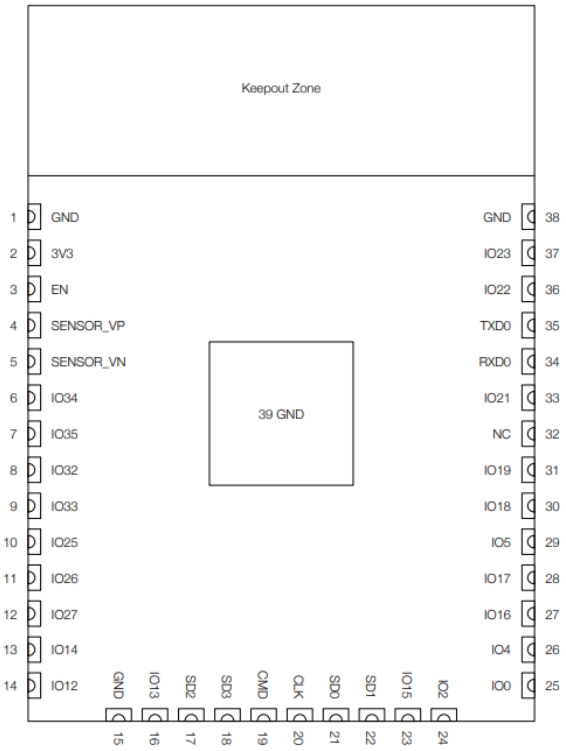
Categories	Items	Specifications
Certification	RF certification	FCC/CE-RED
	Green certification	RoHS/REACH
Test	Reliability	HTOL/HTSL/uHAST/TCT/ESD
Wi-Fi	Protocols	802.11 b/g/n (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μs guard interval support
	Frequency range	2.4 ~ 2.5 GHz
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and BLE specification
	Radio	NZIF receiver with –97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module Interface	SD card, UART, SPI, I2C, GPIO, ADC, DAC
	Integrated Crystal	40 MHz
	Integrated SPI Flash	16 MB
	Operating Power Supply	3.0 V ~ 3.6 V
	Operating Current	Average: 80 mA
	Minimum current delivered by power supply	500 mA
	Operating Temperature range	–40 °C ~ +85 °C
	Package size	(18.00±0.10) mm × (25.50±0.10) mm × (3.10±0.10) mm
	Moisture sensitivity level (MSL)	Level 3
	Crypto Chip	Microchip ATECC608A

PinMap

Zerynth Module ZM1 Pin Layout

Features	ESP name	pin number		ESP name	Features
-	Gnd	1	38	Gnd	-
-	3v3	2	37	GPIO23	MDC (Ethernet)
-	En	3	36	GPIO22	EMAC_TXD1 (Ethernet)
(SERIAL2) RX2	GPI36	4	35	GPIO1	TX0 (SERIAL0)
-	GPI39	5	34	GPIO3	RX0 (SERIAL0)
(SERIAL1) RX1	GPI34	6	33	GPIO21	EMAC_TX_EN (Ethernet)
-	GPI35	7	32	NC	-
(SERIAL2) TX2	GPIO32	8	31	GPIO19	EMAC_TXD0 (Ethernet)
(SERIAL2) RTS2	GPIO33	9	30	GPIO18	MDIO (Ethernet)
(Ethernet) EMAC_RXD0	GPIO25	10	29	GPIO5	RTS1 (SERIAL1)
(Ethernet) EMAC_RXD1	GPIO26	11	28	GPIO17	I2C SCL (I2C0)
(Ethernet) EMAC_RX_CRS_DV	GPIO27	12	27	GPIO16	I2C SDA (I2C0)
(SPI0) SCK	GPIO14	13	26	GPIO4	TX1 (SERIAL1)
(SPI0) MISO	GPIO12	14	25	GPIO0	EMAC_CLKIN (Ethernet)
-	Gnd	15	24	GPIO2	CTS2 (SERIAL2)
(SPI0) MOSI	GPIO13	16	23	GPIO15	-
(Reserved) FLASH_D2	GPIO9	17	22	GPIO8	FLASH_D1 (Reserved)
(SERIAL1) CTS1	GPIO10	18	21	GPIO7	FLASH_D0 (Reserved)
(Reserved) FLASH_CS	GPIO11	19	20	GPIO6	FLASH_CLK (Reserved)
		39			
		Gnd - Thermal pad			

Note1: Green Cells are related to pins with fixed exposed functionalities.
Note2: GPI (34, 35, 36, 39) pins are only input pins and can be used as interrupt/ADC.
Note3: GPIO0, GPIO18, GPIO19, GPIO21, GPIO22, GPIO23, GPIO25, GPIO26, GPIO27 are related to ethernet connectivity.
Note3: GPIO5, GPIO10, GPIO2, GPIO33 are related to hardware flow control for SERIAL1,SERIAL2.
Note4: The development board supports up to 3 attached expansion boards.



Zerynth Pin Mapping

Virtual pins in ZSDK are mapped exactly as the hardware pins, for instance:
D0 is the GPIO0 and D39 is the GPI39.

Bootstrap pins

ZM1 has five strapping pins, which can be seen in the layout:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register ”GPIO_STRAPPING”.
During the chip’s system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of ”0” or ”1”, and hold these bits until the chip is powered down or shut down.
The strapping bits configure the device’s boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.
To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU’s GPIOs to control the voltage level of these pins when powering on ESP32.
After reset release, the strapping pins work as normal-function pins.

VOltage of Internal LDO (VDD_SDIO)			
PIN	**Default**	**3.3V**	**1.8V**
MTDI	Pull-down	0	1
Booting Mode			
PIN	Default	SPI BOOT	Download Boot
GPIO0	Pull-up	1	0
GPIO2	Pull-down	Don't Care	0
Enabling/Disabling Debugging Log Print over U0TXD During Booting			
PIN	Default	U0TXD Active	U0TXD Silent
MTDO	Pull-up	1	0

Timing of SDIO Slave					
PIN	Default	FE Sampling FE Output	FE Sampling FE OUTPUT	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Peripherals Overview

- 22 GPIOs and 4 GPIs
- 12-bit SAR ADC to 8 channels
- 1 SPI peripheral enabled
- 1 I2C peripheral enabled
- 3 UART instances enabled (2 with support for hardware flow control)
- Ethernet MAC interface with dedicated DMA and IEEE 1588 support
- 8 PWMs enabled channels

Functional Description

CPU and Internal Memory

ESP32-D0WD contains a dual-core Xtensa® 32-bit LX6 MCU. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor
- during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining
- 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

Crystal Oscillators

The module uses a 40-MHz crystal oscillator.

Power-supply

Please refer to the ESP32 Technical reference manual.

Peripherals

GPIO

ESP32 has 22 GPIO pins which can be assigned various functions by programming the appropriate registers.

Most of the digital GPIOs can be configured as internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts.

Most of the digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control.
These pins can be multiplexed with other functions, such as the UART, SPI, etc.

Analog to Digital Converter (ADC)

ZM1 integrates 12-bit SAR ADCs .With appropriate settings, the ADCs can be configured to measure voltage on 8 pins maximum.

Parameter	Description	Min	Max	Unit
DNL (Differential nonlinearity)	RTC controller, ADC connected to an external 100 nF capacitor; DC signal input ambient temperature at 25 C. Wi-FI%BT off	-7	7	LSB
INL (Integral nonlinearity)		-12	12	LSB
Sampling rate	RTC controller	-	200	ksps
	DIG controller	-	2	Msps

Notes:

- When atten=3 and the measurement result is above 3000 (voltage at approx. 2450 mV), the ADC accuracy will be worse than described in the table above.
- To get better DNL results, users can take multiple sampling tests with a filter, or calculate the average value.
- The input voltage range of GPIO pins within VDD3P3_RTC domain should strictly follow the DC characteristics provided. Otherwise, measurement errors may be introduced, and chip performance may be affected.

By default, there are ±6% differences in measured results between chips.

For more information on ADC in Zerynth SDK, please refer to the online documentation.

Universal Asynchronous Receiver Transmitter (UART)

ZM1 has three UART interfaces, which provide asynchronous communication, communicating at a speed of up to 5 Mbps. UART provides hardware flow control thanks to the management of the CTS and RTS signals.
For more information on UART in the Zerynth SDK, please refer to the online documentation.

I2C Interface

ZM1 has one I2C bus interface.
The I2C interfaces support:

- Standard mode (100 Kbit/s)
- Fast mode (400 Kbit/s)
- Fast mode Plus (1 Mbit/s)
- Up to 5 MHz, yet constrained by SDA pull-up strength
- 7-bit/10-bit addressing mode
- Dual addressing mode

For more information on I2C in Zerynth SDK, please refer to the online documentation.

Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) controller can be used for driving digital motors and smart lights. For more information on PWM in Zerynth SDK, please refer to the online documentation.

Serial Peripheral Interface (SPI)

ZM1 features one SPI in slave and master modes in 1-line full-duplex and 1/2/4-line half-duplex communication modes. These SPIs also support the following general-purpose SPI features:

- Four modes of SPI transfer format, which depend on the polarity (CPOL) and the phase (CPHA) of the SPI clock
- Up to 80 MHz (The actual speed it can reach depends on the selected pads, PCB tracing, peripheral characteristics, etc.)

For more information on SPI in Zerynth SDK, please refer to the online documentation.

Timers and Watchdogs

Timers and Watchdogs are supported by Zerynth SDK, For more information on timers please refer to the online documentation.

Security

The ATECC608A is a member of the Microchip CryptoAuthentication™ family of high-security cryptographic devices which combine world-class hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols.

Electrical Characteristics

Absolute Maximum rating:

Stresses beyond the absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Symbol	Parameter	Min	Max	Unit
VDD33	VDD33 Power supply voltage	–0.3	3.6	V
Ioutput	Cumulative IO output current	-	1,100	mA
Tstore	Storage temperature	-40	150	°C

Recommended Operating Conditions:

Stresses beyond the absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	VDD33 Power supply voltage	3.0	3.3	3.6	V
Ivdd	Current delivered by external power supply	0.5	-	-	A
T	Operating temperature	-40	-	85	°C

DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typical	Max	Unit
CIN	Pin capacitance		-	2	-	pF
VIH	High-level input voltage		0.75×VDD	-	VDD1+0.3	V
VIL	Low-level input voltage		–0.3	-	0.25×VDD	V
IIH	High-level input current		-	-	50	nA
IIL	Low-level input current		-	-	50	nA
VOH	High-level output voltage		0.8×VDD	-	-	V
VOL	Low-level output voltage		-	-	0.1×VDD	V
IOH	High-level source current (VDD1 = 3.3 V, VOH >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain	-	40	-	mA
		VDD3P3_RTC power domain	-	40	-	mA
		VDD_SDIO power domain	-	20	-	mA
IOL	Low-level sink current (VDD1 = 3.3 V, VOL = 0.495 V, output drive strength set to the maximum)		-	28	-	mA
RPu	Resistance of internal pull-up resistor		-	45	-	kΩ
RPD	Resistance of internal pull-down resistor		-	45	-	kΩ
VIL_nRST	Low-level input voltage of CHIP_PU to power off the chip		-	-	0.6	V

Wifi Radio

Parameter	Mode	Min	Typ	Max	Unit
Operating frequency range	-	2412	-	Mhz	V
Output Impedance	-	-	See note 2	-	Ω
TX power	11n, MCS7	12	13	14	dBm
	11b mode	18.5	19.5	20.5	dBm
Sensitivity	11b, 1 Mbps	-	-97	-	dBm
	11b, 11 Mbps	-	–87	-	dBm
	11g, 6 Mbps	-	–92	-	dBm
	11g, 54 Mbps	-	-74	-	dBm
	11n, HT20, MCS0	-	-91	-	dBm
	11n, HT20, MCS7	-	-71	-	dBm
	11n, HT40, MCS0	-	-89	-	dBm
	11n, HT40, MCS7	-	-69	-	dBm
Adjacent channel rejection	11g, 6 Mbps	-	31	-	dB
	11g, 54 Mbps	-	14	-	dB
	11n, HT20, MCS0	-	31	-	dB
	11n, HT20, MCS7	-	13	-	dB

- Devices should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.
- For the modules that use IPEX antennas, the output impedance is 50 Ω. For other modules without IPEX antennas, users do not need to be concerned about the output impedance.
- Target TX power is configurable based on device or certification requirements.

Bluetooth: Receiver

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-	-97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

Bluetooth: Transmitter

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	-12	-	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	-	-52	-	dBm
	F = F0 ± 3 MHz	-	-58	-	dBm
	F = F0 ± > 3 MHz	-	-60	-	dBm
Δ f1avg	-	-	-	265	kHz
Δ f2max	-	247	-	-	kHz
Δ f2avg/Δ f1avg	-	-	-0.92	-	-
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 µs
Drift	-	-	2	-	kHz

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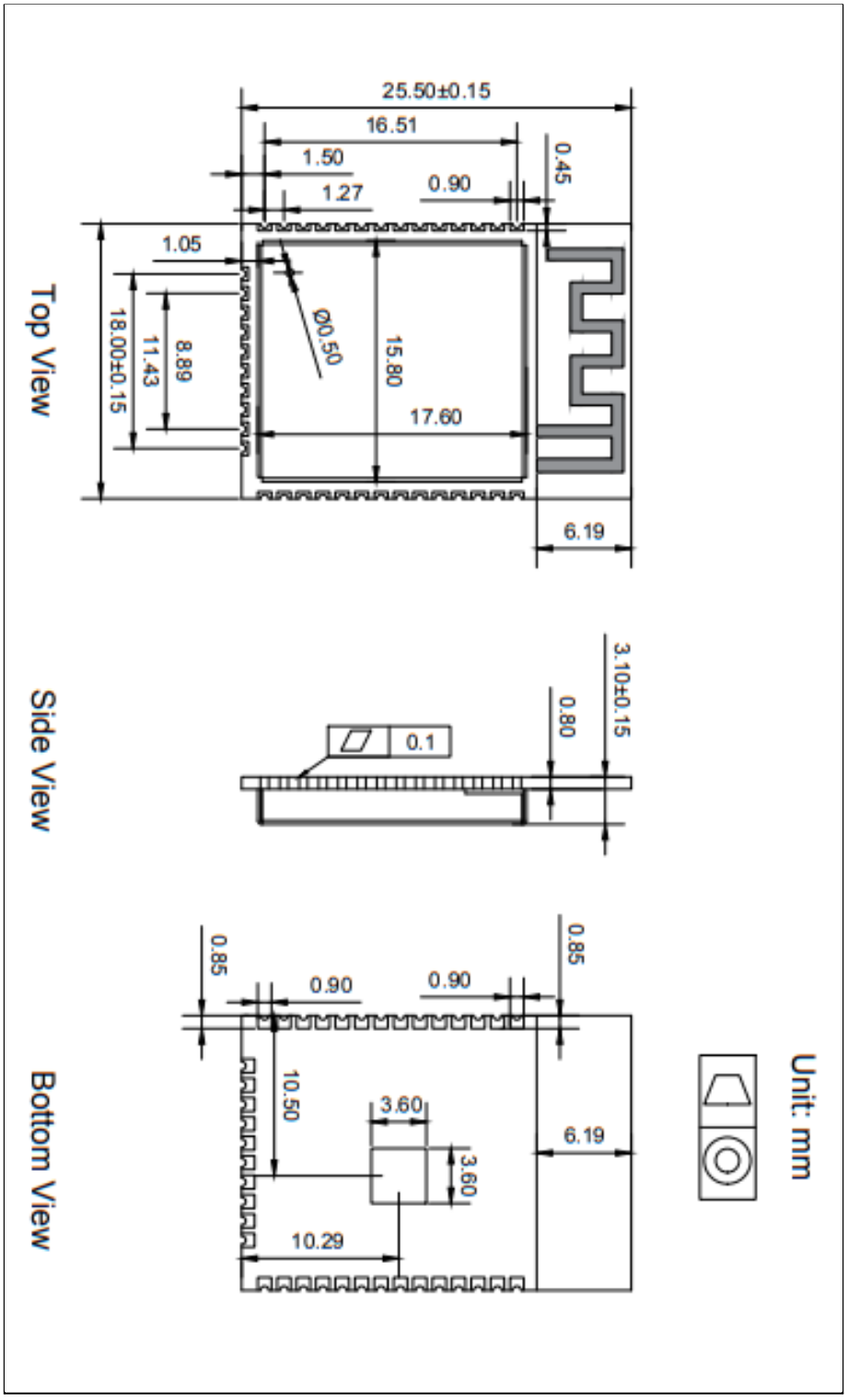
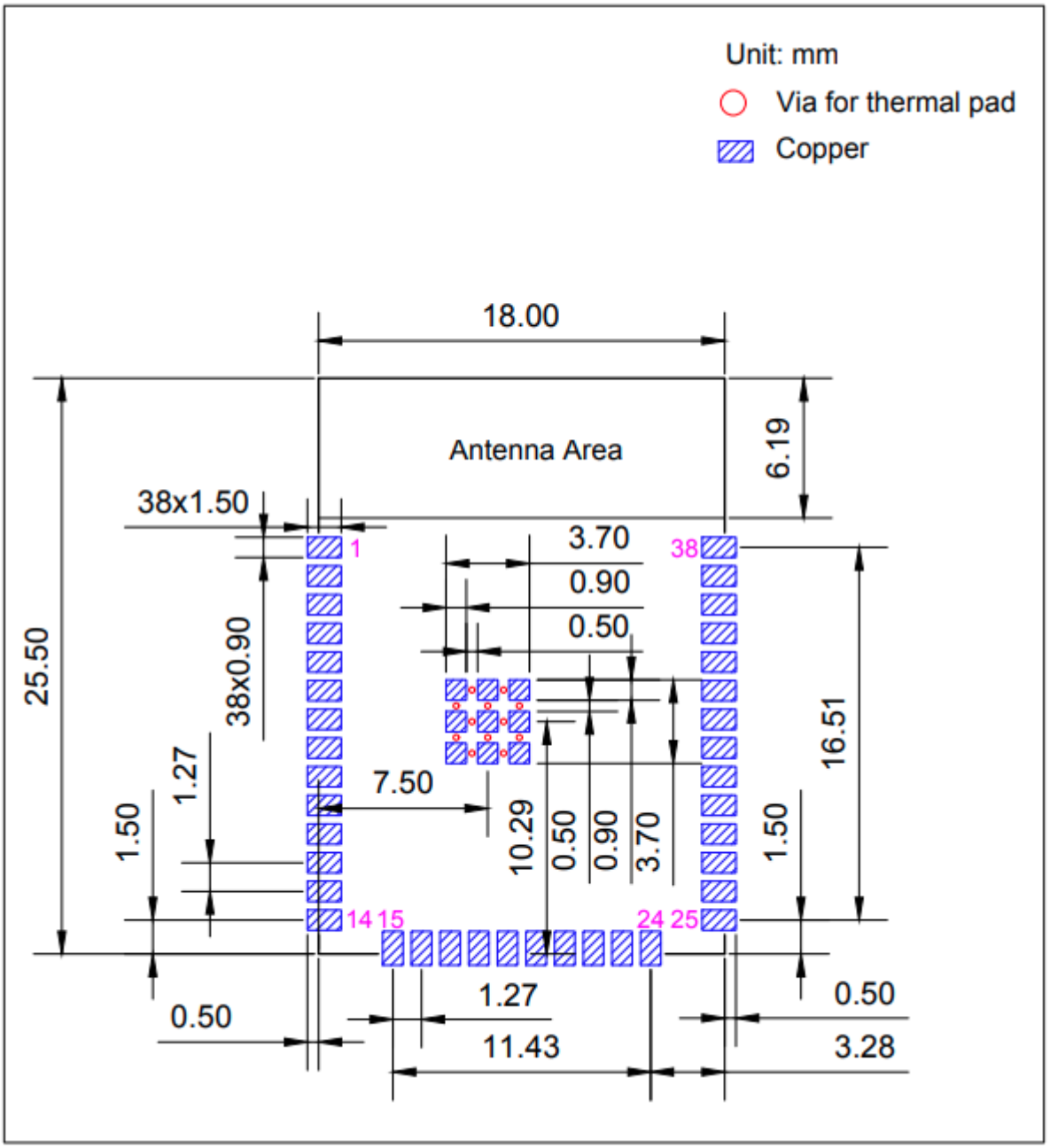
Physical Dimensions



PCB Footprint



Note: Dimensions are in mm

Zerynth SDK

Zerynth platform is designed to simplify and accelerate the development of IoT applications. Zerynth offers tools for developers, system integrators, and businesses to enable IoT for their products, rapidly in a secure and connected way.

Zerynth SDK is the official development framework for Zerynth hardware, It includes a compiler, device drivers and libraries drivers, In addition to simple tutorials, example codes, and application examples.

Zerynth SDK and all the required libraries can be installed on Windows, Linux and Mac using the Zerynth Installer (https://www.zerynth.com/zsdk).

Resources

- Zerynth Online Documentation
  www.docs.zerynth.com
- Zerynth Website
  www.zerynth.com
  Click on the following links to access documents related to ESP32.