MPXV7007

Integrated silicon pressure sensor, on-chip signal conditioned, temperature compensated and calibrated

Rev. 4 — 26 January 2021 Product data sheet

1 General description

The MPXV7007 series piezoresistive transducers are monolithic silicon pressure sensors. The MPXV7007 is designed for a wide range of applications, particularly applications employing a microcontroller, or microprocessor with analog-to-digital inputs. This transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high-level analog output signal that is proportional to the applied pressure.

2 Features and benefits

- Ideally suited for microprocessor or microcontroller-based systems
- Temperature compensated over –40 °C to +125 °C
- Thermoplastic (PPS) surface mount package
- Patented silicon shear stress strain gauge
- Available in differential and gauge configurations

3 Applications

- Hospital beds
- HVAC
- Respiratory systems
- Process control

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MPXV7007DP	SO8	Plastic, small outline package, 8 terminals, 2.54 mm pitch, 12.06 mm x 12.06 mm x 7.62 mm body	SOT1693-1
MPXV7007GC6U	SO8	Plastic, small outline package, 8 terminals, 2.54 mm pitch, 10.67 mm x 10.67 mm x 12.96 mm body	SOT1854-1
MPXV7007GP	SO8	Plastic, small outline package, 8 terminals, 2.54 mm pitch, 12.06 mm x 12.06 mm x 8.38 mm body	SOT1693-3

4.1 Ordering options

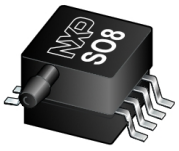
Table 2. Ordering options

Device name	Package options	SOT no.	# of Ports			Pressure type			Device marking
			None	Single	Dual	Gauge	Differential	Absolute	
Small Outline Package									
MPXV7007DP	Trays	1693-1			•		•		MPXV7007DP
MPXV7007DPT1	Tape and Reel	1693-1			•		•		MPXV7007DP
MPXV7007GC6U	Rails	1854-1		•		•			MPXV7007G
MPXV7007GC6T1	Tape and Reel	1854-1		•		•			MPXV7007G
MPXV7007GP	Trays	1693-3		•		•			MPXV7007GP

Small outline packages

MPXV7007DP/DPT1
CASE 1351-01
SOT1693-1

MPXV7007GC6U/C6T1
CASE 482A-01
SOT1854-1



MPXV7007GP
CASE 1369-01
SOT1693-3

5 Block diagram

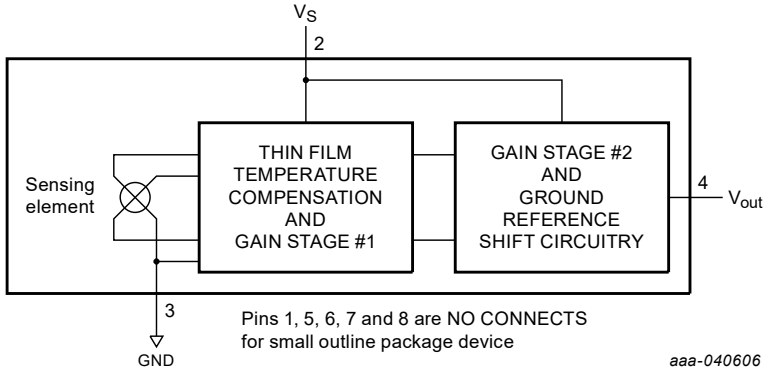


Figure 1. Integrated pressure sensor schematic

6 Pinning information

6.1 Pinning

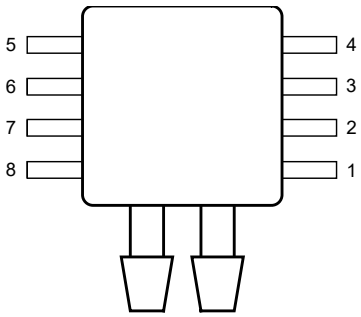


Figure 2. MPXV7007DP/DPT1 pin diagram

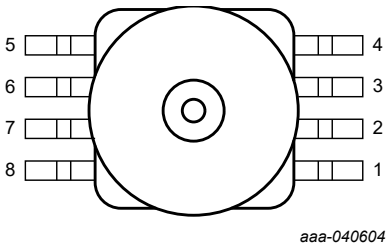


Figure 3. MPXV7007GC6U/C6T1 pin diagram

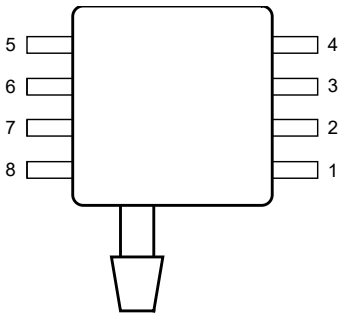


Figure 4. MPXV7007GP pin diagram

6.2 Pin description

This device family uses the style 2 pin configuration documented in Table 3 and shown in Figure 12.

Table 3. Pin description

Symbol	Pin[1]	Description
n.c.	1	—[2]
V_S	2	Supply voltage
GND	3	Ground
V_{out}	4	Voltage output
n.c.	5	—[2]
n.c.	6	—[2]
n.c.	7	—[2]
n.c.	8	—[2]

[1] The notch in the lead indicates pin 1.
[2] Internal device connection. Do not connect to external circuitry or ground

7 Maximum ratings

Table 4. Maximum ratings[1]

Rating	Symbol	Value	Unit
Maximum pressure	P_{max}	75	kPa
Storage temperature	T_{stg}	–40 to +125	°C
Operating temperature	T_A	–40 to +125	°C

[1] Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

8 Operating characteristics

Table 5. Operating characteristics)

(V_S = 5.0 Vdc, T_A = 25 °C unless otherwise noted. Decoupling circuit shown in Figure 6 required to meet specification.

Characteristic	Symbol	Min	Typ	Max	Unit
Pressure range[1]	P_{OP}	–7	—	7	kPa
Supply voltage[2]	V_S	4.75	5.0	5.25	Vdc
Supply current	I_o	—	7.0	10	mAdc
Minimum pressure offset[3] (0 °C to 85 °C) @ V_S = 5.0 Volts	V_{off}	0.33	0.5	0.67	Vdc
Full scale output[4] (0 °C to 85 °C) @ V_S = 5.0 Volts	V_{FSO}	4.3	4.5	4.7	Vdc
Full scale span[5] (0 °C to 85 °C) @ V_S = 5.0 Volts	V_{FSS}	—	4.0	—	Vdc
Accuracy[6] (0 °C to 85 °C)	—	—	—	±5.0	%V_{FSS}
Sensitivity	V/P	—	286	—-	mV/kPa
Response time[7]	t_R	—	1.0	—-	ms
Output source current at full scale output	I_{O+}	—	0.1	—-	mAdc
Warm-up time[8]	—	—	20	—-	ms
Offset stability[9]	—	—	± 0.5	—-	%V_{FSS}

[1] 1.0 kPa (kiloPascal) equals 0.145 psi.
[2] Device is ratiometric within this specified excitation range.
[3] Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
[4] Full scale output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.
[5] Full scale span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
[6] Accuracy (error budget) consists of the following:
- Linearity: Output deviation from a straight-line relationship with pressure over the specified pressure range.
- Temperature hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
- Pressure hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25 °C.
- TcSpan: Output deviation over the temperature range of 0 °C to 85 °C, relative to 25 °C.
- TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 0 °C to 85 °C, relative to 25 °C.
- Variation from nominal: The variation from nominal values, for offset or full scale span, as a percent of V_{FSS}, at 25 °C.

[7] Response time is defined as the time for the incremental change in the output to go from 10 % to 90 % of its final value when subjected to a specified step change in pressure.
[8] Warm-up time is defined as the time required for the product to meet the specified output voltage after the pressure has been stabilized.
[9] Offset stability is the output deviation of the product when subjected to 1000 hours of pulsed pressure, temperature cycling with bias test.

9 Characteristics

9.1 On-chip temperature compensation, calibration, and signal conditioning

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration, and signal conditioning circuitry onto a single monolithic chip.

Figure 5 illustrates the differential or gauge configuration in the basic chip carrier (Case 482). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm.

The MPXV7007 series pressure sensor operating characteristics, and internal reliability and qualification tests are based on use of dry air as the pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.

Figure 6 shows the recommended decoupling circuit for interfacing the integrated sensor to the analog-to-digital input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 7 shows the sensor output signal relative to pressure input. Typical, minimum, and maximum output curves are shown for operation over a temperature range of 0 °C to 85 °C using the decoupling circuit shown in Figure 6. The output saturates outside the specified pressure range.

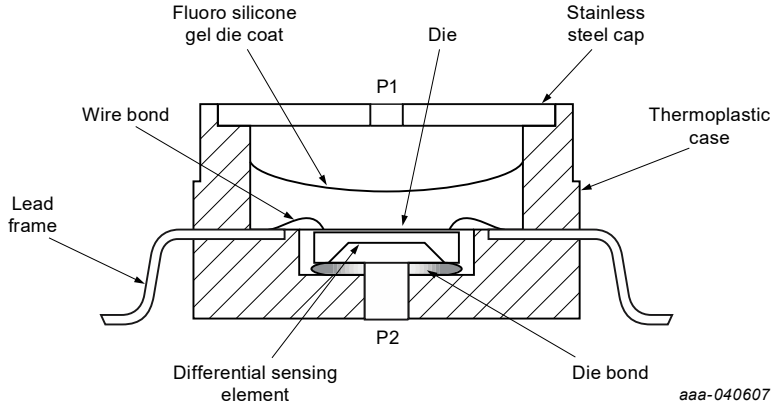


Figure 5. Cross-Sectional Diagram SOP (not to scale)

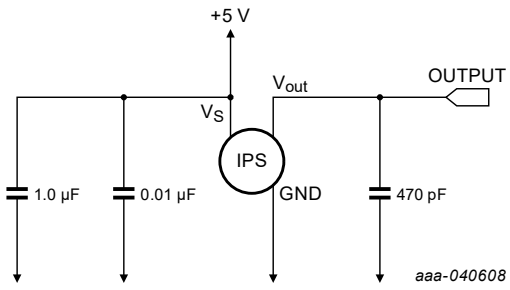


Figure 6. Recommended Power Supply Decoupling and Output Filtering

For additional output filtering, refer to Application Note AN1646[1].

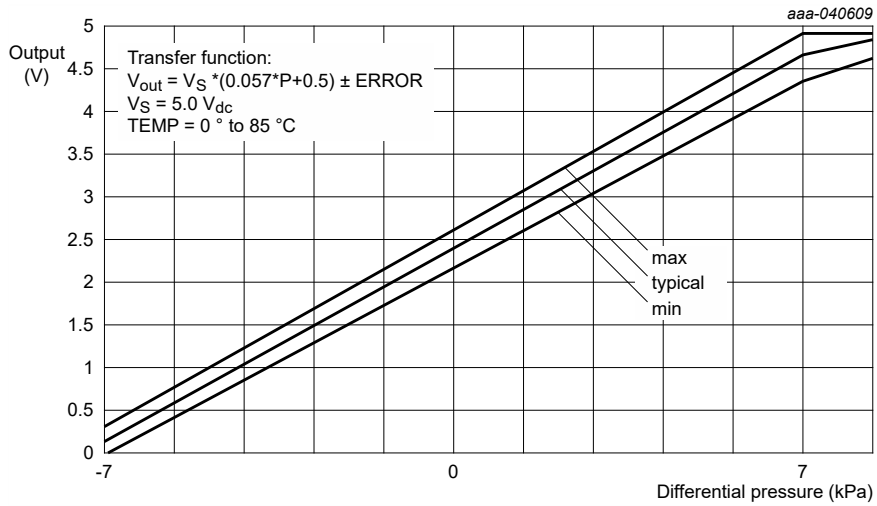


Figure 7. Output versus Pressure Differential

Transfer function

Nominal transfer value:

$$V_{out} = V_S \times (0.057 \times P + 0.5) \pm (\text{Pressure Error} \times \text{Temp. Factor} \times 0.057 \times V_S)$$

$$V_S = 5.0\ V \pm 0.25\ Vdc$$

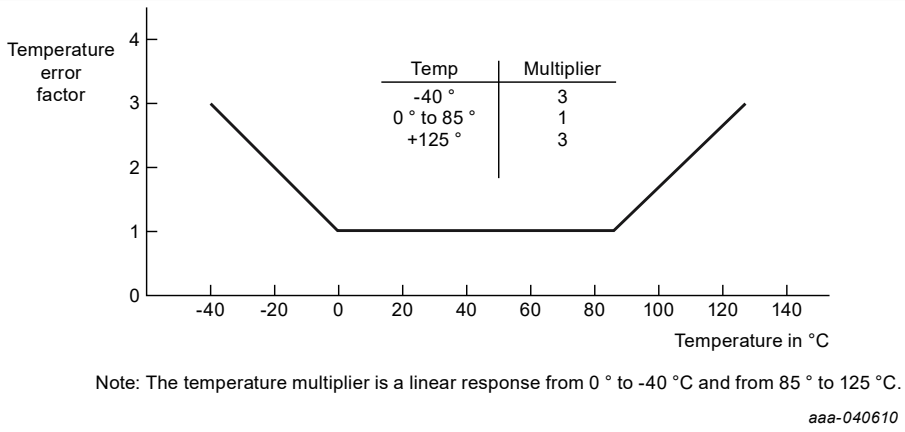


Figure 8. Temperature error band

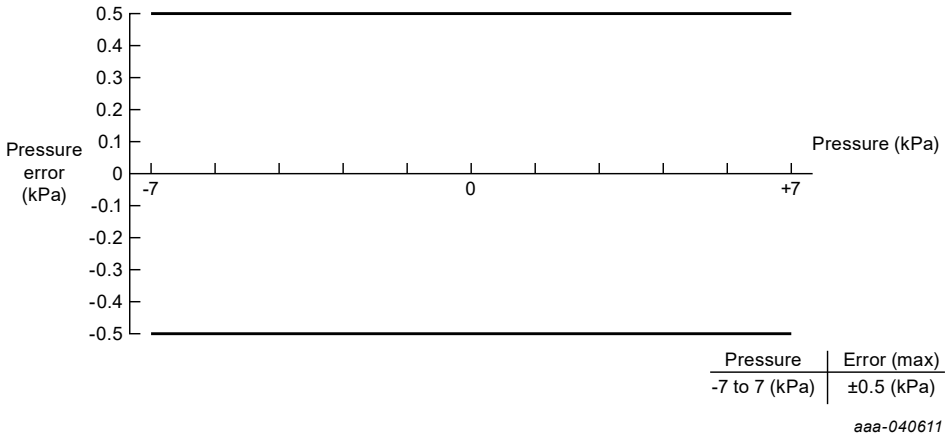


Figure 9. Pressure error band

9.2 Pressure (P1)/Vacuum (P2) side identification table

NXP designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The P1 side is the side containing fluoro silicone gel which protects the die from harsh media. The pressure sensor is designed to operate with both positive and negative differential pressure applied, P1 > P2 or P1 < P2.

The P1 side may be identified by using Table 6.

Table 6. Pressure side identification

Part number	Case type	Pressure (P1) Side identifier
MPXV7007GC6U/C6T1	482A	Side with port attached
MPXV7007GP	1369	Side with port attached
MPXV7007DP/DPT1	1351	Side with part marking

9.3 Minimum recommended footprint for surface-mounted applications

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages self-align when subjected to a solder reflow process. NXP recommends designing boards with a solder mask layer to avoid bridging and shorting between solder pads.

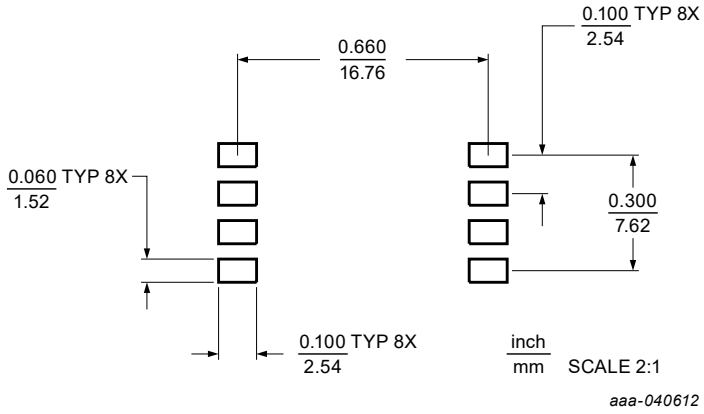
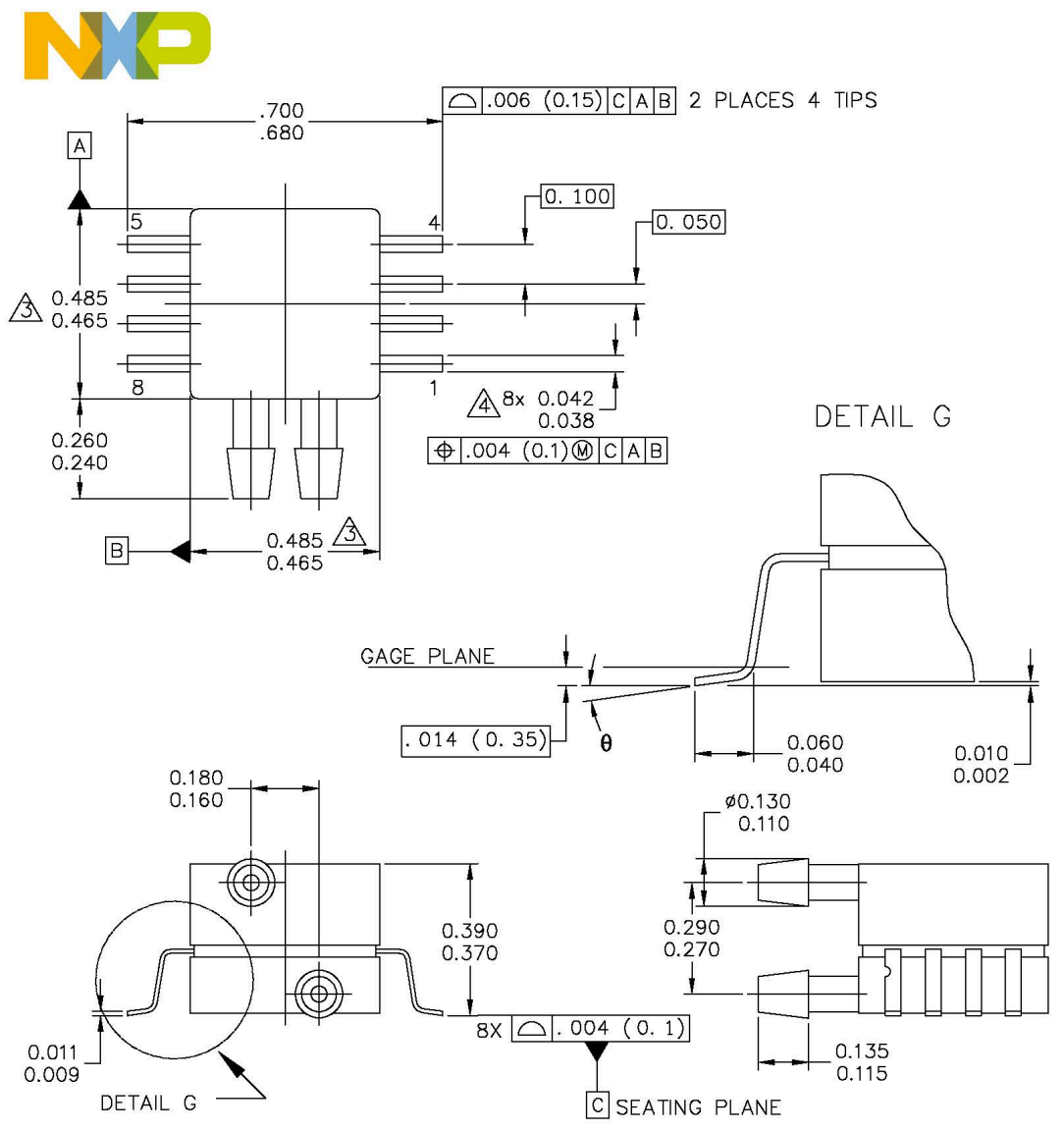


Figure 10. Small Outline Package Footprint

10 Package outline



© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: B
	STANDARD: NON-JEDEC	
	SOT1693-1	14 MAR 2016

Figure 11. SOT1693-1, 8 Lead sensor, dual port package outline, 98ASA99255D, Rev. B

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.
   MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
   PROTRUSION SHALL BE .008 MAXIMUM.

STYLE 1:	STYLE 2:
PIN 1: GND	PIN 1: N/C
PIN 2: +Vout	PIN 2: Vs
PIN 3: Vs	PIN 3: GND
PIN 4: –Vout	PIN 4: Vout
PIN 5: N/C	PIN 5: N/C
PIN 6: N/C	PIN 6: N/C
PIN 7: N/C	PIN 7: N/C
PIN 8: N/C	PIN 8: N/C

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: B
	STANDARD: NON–JEDEC	
	SOT1693–1	14 MAR 2016

Figure 12. SOT1693-1, 8 Lead sensor, dual port package outline notes, 98ASA99255D, Rev. B

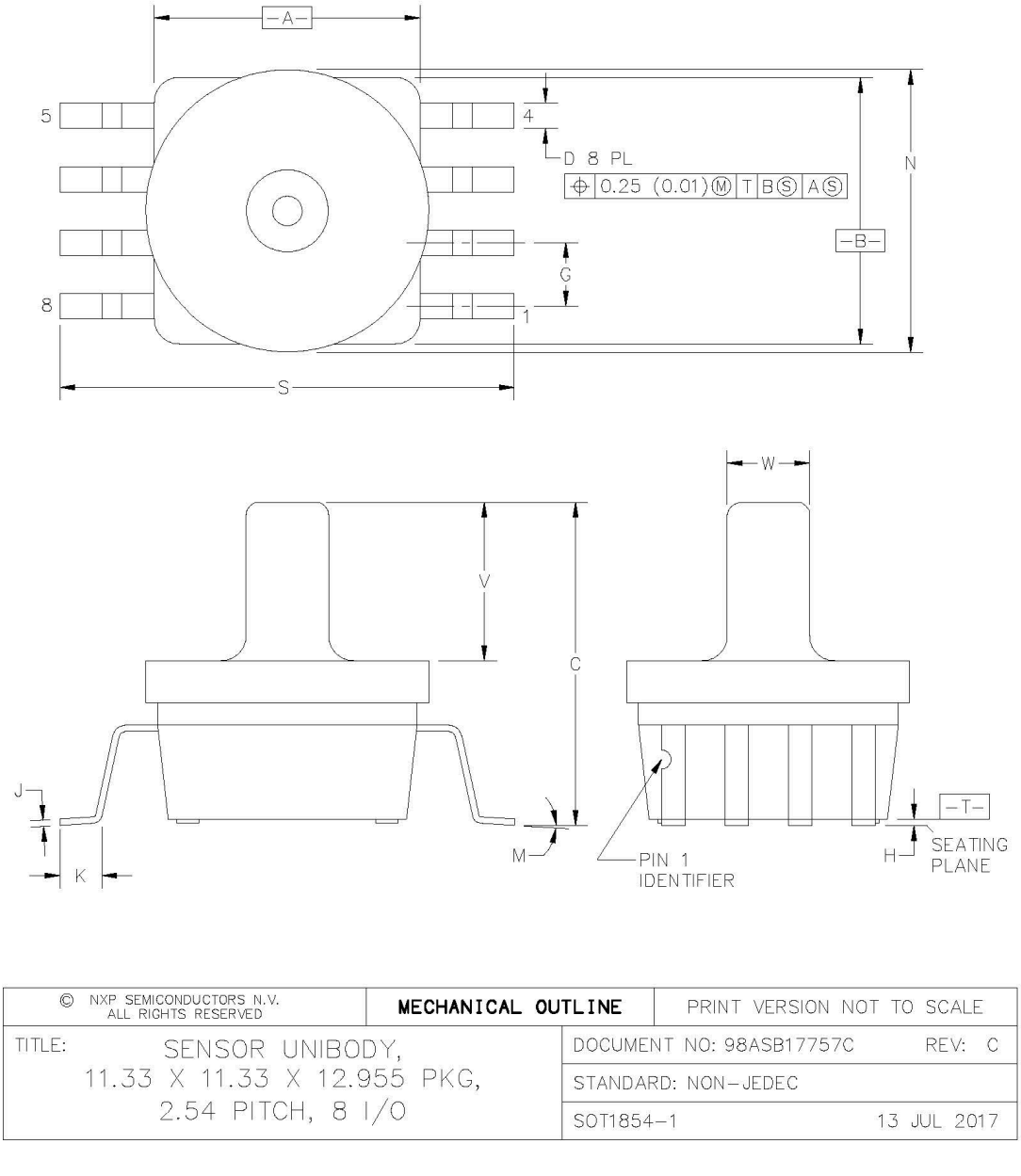


Figure 13. SOT1854-1, Unibody sensor package outline, 98ASB17757C, Rev. C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION 'A' AND 'B' DO NOT INCLUDE MOLD PROTUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

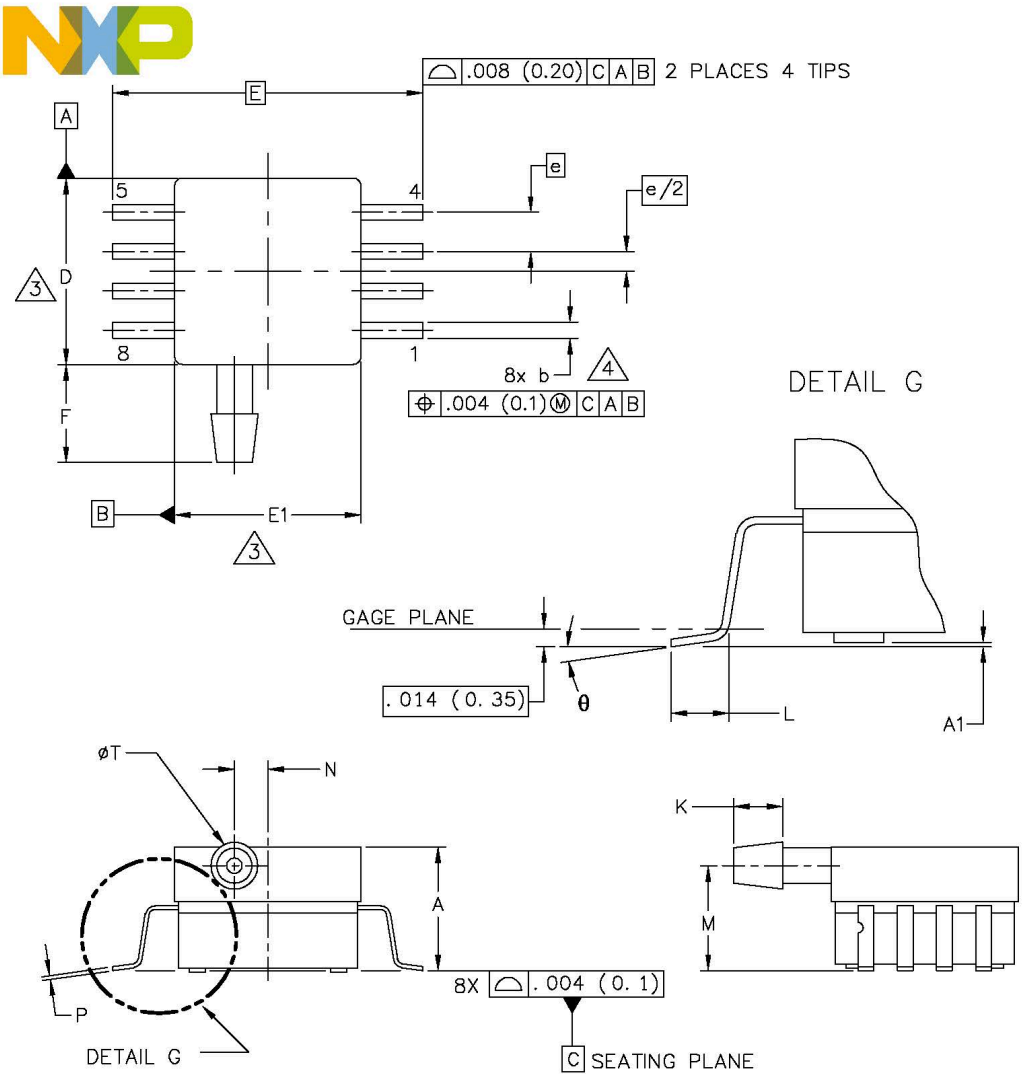
TITLE: SENSOR UNIBODY, 11.33 X 11.33 X 12.955 PKG, 2.54 PITCH, 8 I/O

DOCUMENT NO: 98ASB17757C REV: C

STANDARD: NON–JEDEC

SOT1854–1 13 JUL 2017

Figure 14. SOT1854-1, Unibody sensor package outline notes, 98ASB17757C, Rev. C



© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SOP, SIDE PORT	DOCUMENT NO: 98ASA99303D	REV: E
	STANDARD: NON-JEDEC	
	SOT1693-3	14 MAR 2016

Figure 15. SOT1693-3, 8 Lead SOP, Side port package out line, 98ASA99303D, Rev. E

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.300	.330	7.62	8.38	θ	0°	7°	0°	7°
A1	.002	.010	0.05	0.25	–	---	---	---	---
b	.038	.042	0.96	1.07	–	---	---	---	---
D	.465	.485	11.81	12.32	–	---	---	---	---
E	.717 BSC		18.21 BSC		–	---	---	---	---
E1	.465	.485	11.81	12.32	–	---	---	---	---
e	.100 BSC		2.54 BSC		–	---	---	---	---
F	.245	.255	6.22	6.47	–	---	---	---	---
K	.120	.130	3.05	3.30	–	---	---	---	---
L	.061	.071	1.55	1.80	–	---	---	---	---
M	.270	.290	6.86	7.36	–	---	---	---	---
N	.080	.090	2.03	2.28	–	---	---	---	---
P	.009	.011	0.23	0.28	–	---	---	---	---
T	.115	.125	2.92	3.17	–	---	---	---	---

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:
8 LD SOP, SIDE PORT

DOCUMENT NO: 98ASA99303D REV: E
STANDARD: NON–JEDEC
SOT1693–3 14 MAR 2016

Figure 16. SOT1693-3, 8 Lead SOP, Side port package out line notes, 98ASA99303D, Rev. E

11 References

[1] AN1646 – Noise considerations for integrated pressure sensors
https://www.nxp.com/docs/en/application-note/AN1646.pdf

12 Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MPXV7007 v.4	20210126	Product data sheet	—	MPXV2050 v.3
Modifications	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors, N.V. Legal texts have been adapted to the new company name where appropriate. • Global changes, revised as follows: – Revised all images including the package outline drawings to comply with NXP Semiconductor graphic standards. – Performed minor grammatical, content, and typographical changes throughout. • Section 1, revised the first paragraph. • Section 2, removed bullet "5.0 % maximum error over 0 °C to 85 °C". • Section 6.2, added clarification stating this device family uses the style 2 pin configuration as shown in Figure 12. • Section 11, added new reference section.			
MPXV7007 v.3	201210	Product data sheet	—	MPXV7007 v.2
Modifications	• Deleted references to device numbers MPXV7007G6T1/U, MPXV7007G6U/T1, and MPXV7007GPT1 throughout the document, deleted Case 482-01 Issue O Small Outline Package diagram on page 7.			

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without

limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Integrated silicon pressure sensor, on-chip signal conditioned, temperature compensated and calibrated

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 January 2021
Document identifier: MPXV7007