

AN6328, AN6328S

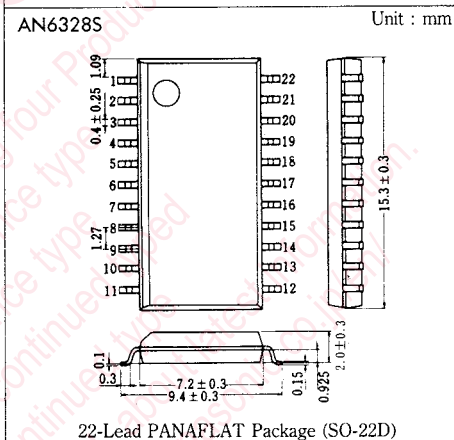
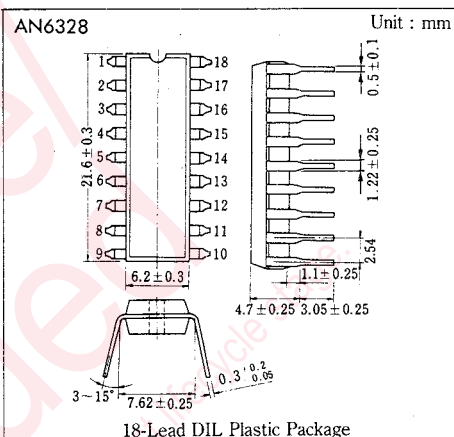
VTR Line Noise Canceller Circuits

■ Outline

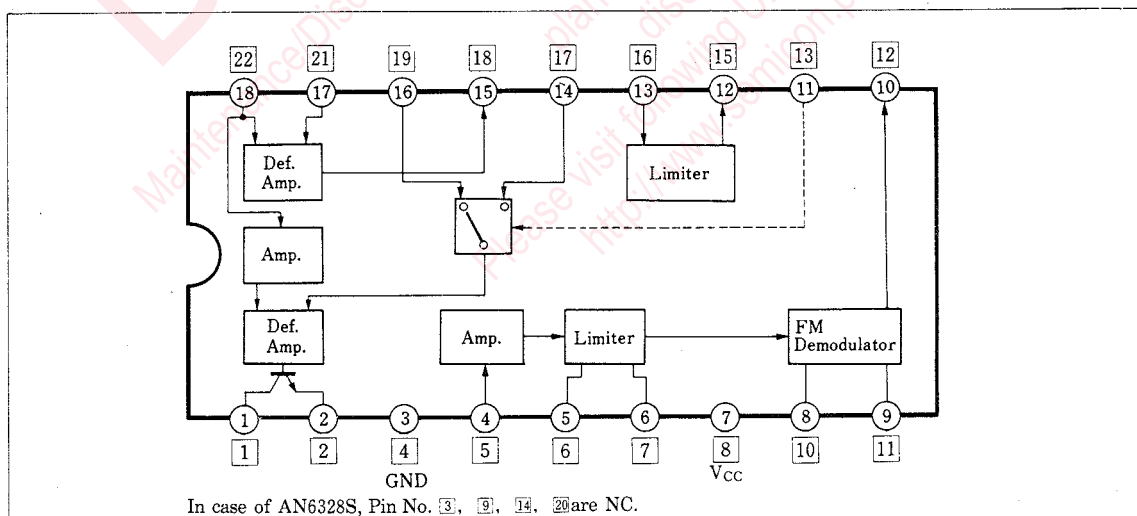
The AN6328 and the AN6328S are integrated circuits designed for VTR's line noise canceller.

■ Features

- The functions consist of:
FM demodulator
Differential amplifier
- Supply voltage: 5V



■ Block Diagram



■ Absolute Maximum Ratings (T_a=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	6.0	V
Power dissipation ($T_a=70^{\circ}\text{C}$)	AN6328	P_D	370	mW
	AN6328S		270*	
Operating ambient temperature		T_{opr}	$-20\sim+70$	$^{\circ}\text{C}$
Storage temperature	AN6328	T_{stg}	$-40\sim+150$	$^{\circ}\text{C}$
	AN6328S		$-40\sim+125$	

* Indicates a package capability

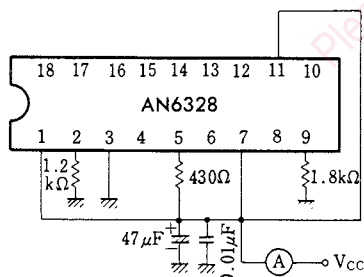
■ Electrical Characteristics (V_{CC}=5V, T_a=25℃±2℃)

Item		Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current	AN6328	I_7	1	Pin⑩ : V_{cc}	30		60	mA
	AN6328S	I_8						
FM demodulator detection sensitivity	AN6328	S_{10}	2	$C=47\text{pF}$, $R_{10}=900\Omega$, $f_{IN}=3.5\sim 4.5\text{MHz}$	80		140	mV/MHz
	AN6328S	S_{12}						
FM demodulator detection limit		f_{lim}	2	$C=47\text{pF}$, $V_{IN}=50\text{mV}_{P-P}$	7.0			MHz
FM demodulator carrier leak	AN6328	CL_{10}	3	$C=47\text{pF}$, $R_{10}=900\Omega$, $f_{IN}=4\text{MHz}$, $V_{IN}=50\text{mV}_{P-P}$			-30	dB
	AN6328S	CL_{12}						
Differential amp. gain (1)	AN6328	G_{V15-1}	4	Input: Pin⑦, $f_{IN}=1\text{MHz}$, $V_{IN}=100\text{mV}_{P-P}$	14.3		17.3	dB
	AN6328S	G_{V18-1}						
Differential amp. gain (2)	AN6328	G_{V15-2}	4	Input: Pin⑧, $f_{IN}=1\text{MHz}$, $V_{IN}=100\text{mV}_{P-P}$	12.8		15.8	dB
	AN6328S	G_{V18-2}						
Main signal amp. system gain		G_{V22-1}	5	Input: Pin⑩, $f_{IN}=1\text{MHz}$, $V_{IN}=100\text{mV}_{P-P}$	10.0		13.0	dB
Mix amp. gain		V_{G17-1}	6	Input: Pin④, $f_{IN}=1\text{MHz}$, $V_{IN}=500\text{mV}_{P-P}$	-4.5		-1.5	dB
Electronic SW select level difference		$V_{O(offset)}$	7	Switching pulse 30kHz			5	mV
Electronic SW select sensitivity	AN6328	S_{11}	8	Switching Pin ① output.			3	V
	AN6328S	S_{13}						
Electronic SW select cross talk(1)		CT_{1-1}	8	Input: Pin④1V _{P-P}			-40	dB
Electronic SW select cross talk(2)		CT_{1-2}	8	Input: Pin⑥1V _{P-P}			-40	dB
Line noise canceller limiter gain	AN6328	G_{V12}	9	$f_{IN}=1\text{MHz}$, $V_{IN}=25\text{mV}_{P-P}$	13.0		17.0	dB
	AN6328S	G_{V15}						

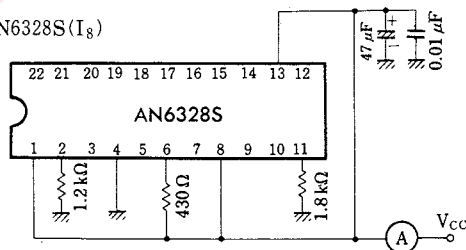
Note) Operating Supply Voltage Range $V_{cc(opr)} = 4.5 \sim 5.5V$

Test Circuit 1

● AN6328 (I₇)

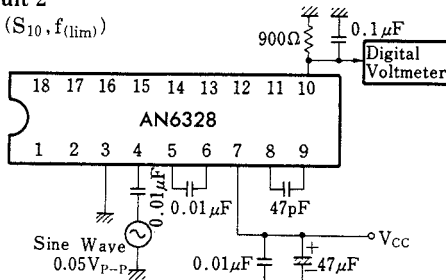


● AN6328S(I₈)



Test Circuit 2

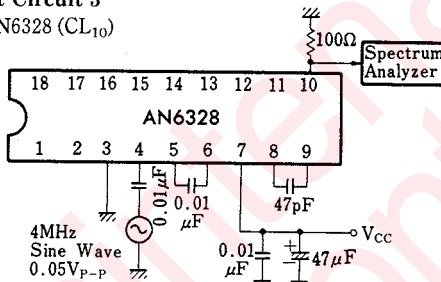
- AN6328 (S_{10}, f_{lim})



- S_{10} Pin⑩ output difference between Pin④ input frequency of 3.5MHz and 4.5MHz
- f_{lim} Pin④ input frequency at which Pin⑩ output is turned linear.

Test Circuit 3

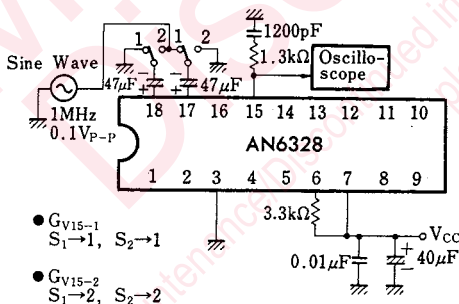
- AN6328 (CL_{10})



- 4MHz component to Pin⑩ output, 8MHz

Test Circuit 4

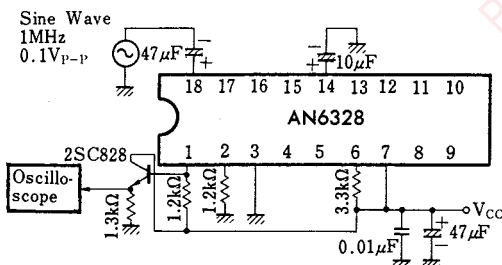
- AN6328 (G_{V15-1}, G_{V15-2})



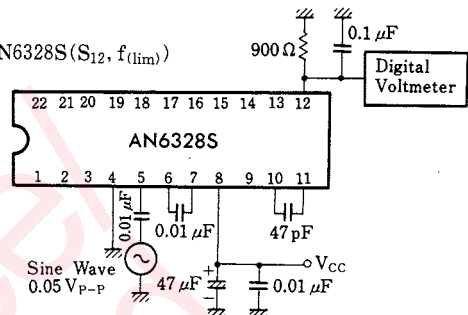
- G_{V15-1} $S_1 \rightarrow 1, S_2 \rightarrow 1$
- G_{V15-2} $S_1 \rightarrow 2, S_2 \rightarrow 2$

Test Circuit 5

- AN6328 (G_{V22-1})

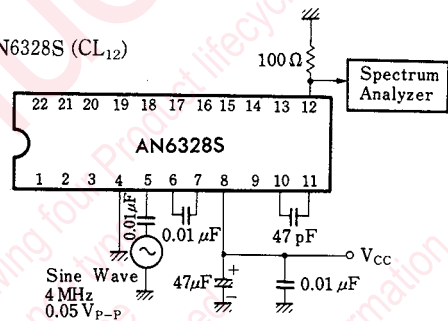


- AN6328S (S_{12}, f_{lim})



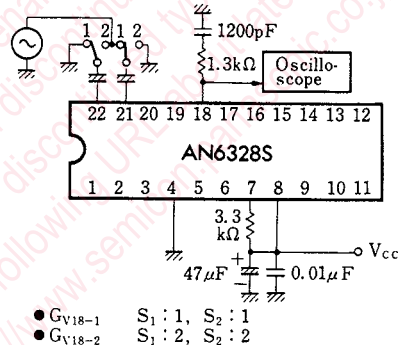
- S_{12} Pin⑫ output difference between Pin⑤ input frequency of 3.5MHz and 4.5MHz
- f_{lim} Pin⑤ input frequency at which Pin⑫ output is turned linear

- AN6328S (CL_{12})



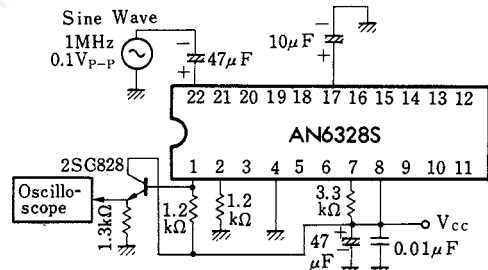
- 4MHz component to Pin⑫ output, 8MHz

- AN6328S (G_{V18-1}, G_{V18-2})

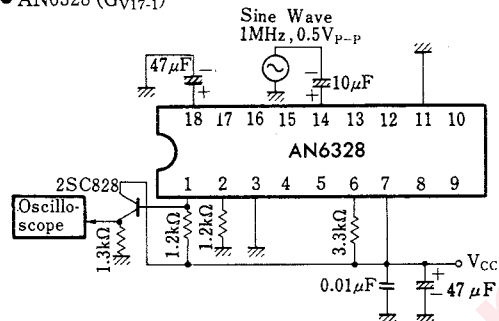
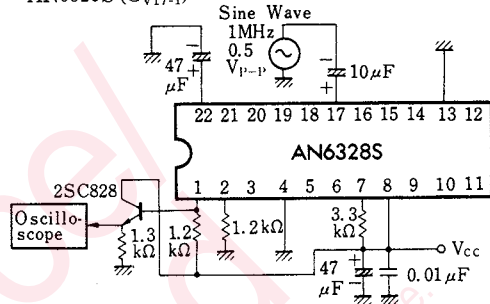


- G_{V18-1} $S_1 : 1, S_2 : 1$
- G_{V18-2} $S_1 : 2, S_2 : 2$

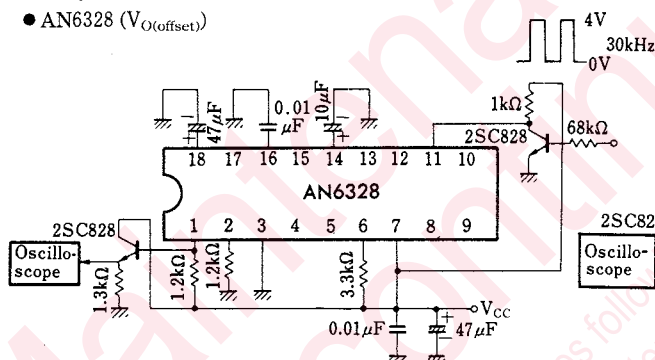
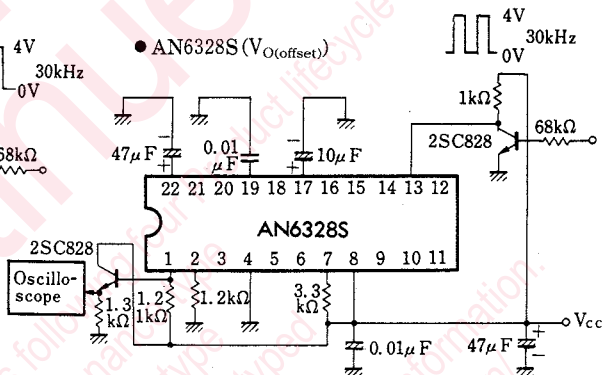
- AN6328S (G_{V22-1})



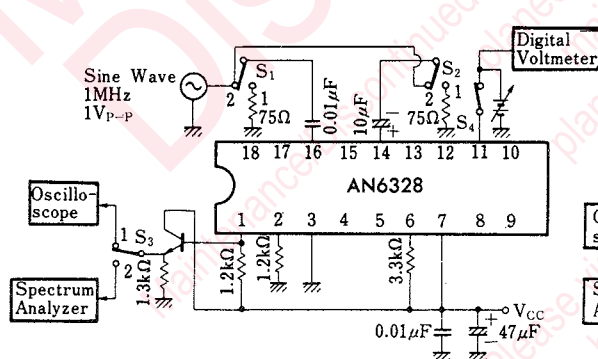
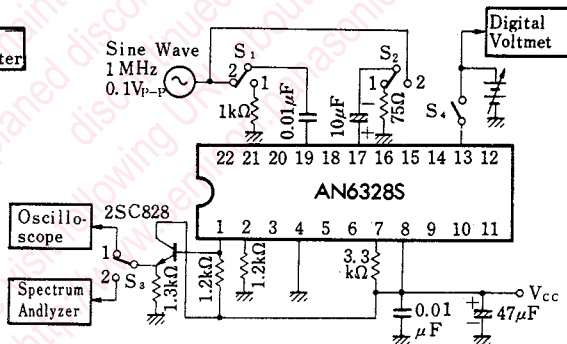
Test Circuit 6

● AN6328 (G_{V17-1})● AN6328S (G_{V17-1})

Test Circuit 7

● AN6328 (V_{O(offset)})● AN6328S (V_{O(offset)})

Test Circuit 8

● AN6328 (S₁₁, CT₁₋₁, CT₁₋₂)● AN6328S (S₁₃, CT₁₋₁, CT₁₋₂)● AN6328 (S₁₁, CT₁₋₁, CT₁₋₂)● S₁₁: S₁→1, S₂→2, S₃→1, S₄→ON

Pin potential when Pin① output is made with Pin⑩ potential decreased from Vcc

● CT₁₋₁: S₁→1, S₂→2, S₃→2, S₄→Vcc

Pin④ output (1MHz component) to Pin⑭ input

● CT₁₋₂: S₁→2, S₂→1, S₃→2, S₄→GND

Pin① output (1MHz component) to Pin⑮ input

● AN6328S (S₁₃, CT₁₋₁, CT₁₋₂)● S₁₃: S₁→1, S₂→2, S₃→1, S₄→ON

Pin⑬ potential when Pin① output is made with Pin⑮ potential is decreased from Vcc

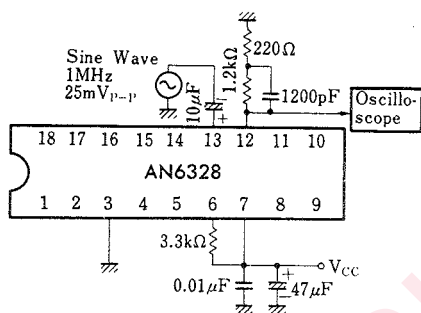
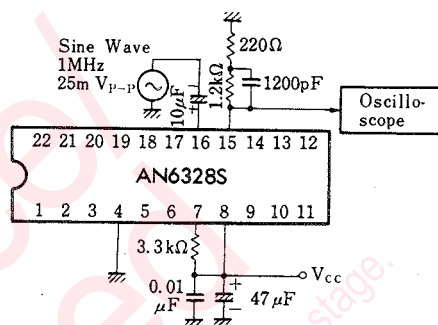
● CT₁₋₁: S₁→1, S₂→2, S₃→2, S₄→ON(Vcc)

Pin① output (1MHz component) to Pin⑰ input

● CT₁₋₂: S₁→2, S₂→1, S₃→2, S₄→OFF(6M)

Pin① output (1MHz component) to Pin⑲ input

Test Circuit 9

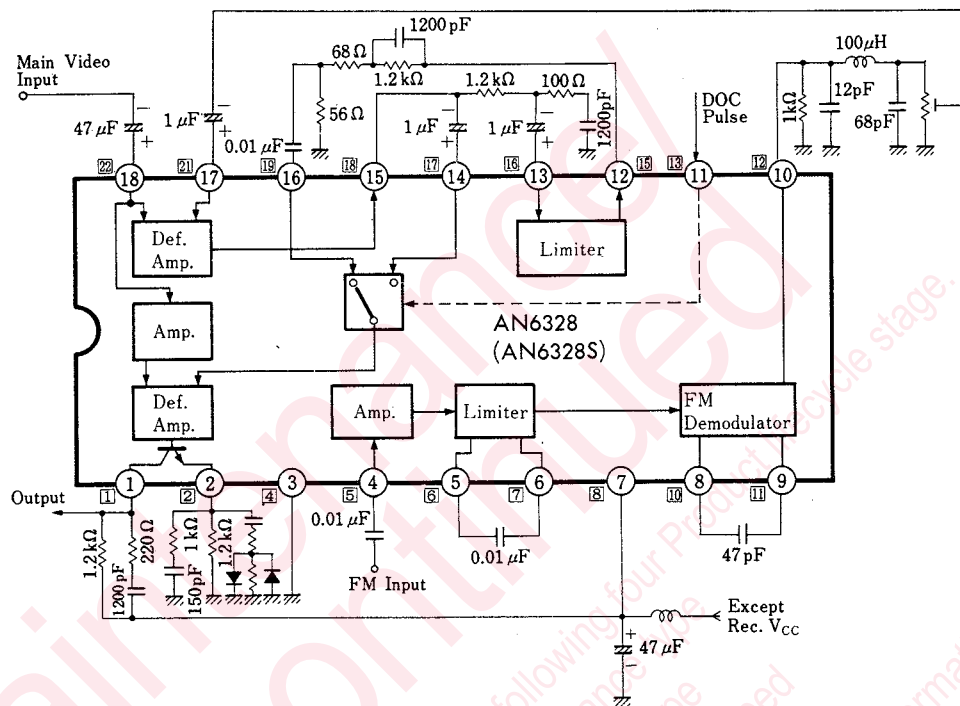
● AN6328 (G_{V12})● AN6328S (G_{V15})

■ Pin

Pin No.	Pin Name		Pin No.	Pin Name	
1 (1)	Line Noise Canceller Output	Collector	10 (12)	FM Demod. Output	
2 (2)		Emitter	11 (13)	DOC Pulse Input	
3 (4)	GND		12 (15)	Line Noise Canceller	Output
4 (5)	1H Delay FM Input		13 (16)	Limiter	Input
5 (6)	FM Limiter	(1)	14 (17)	Electric Switch Input (1)	
6 (7)	Capacitance	(2)	15 (18)	Differential Amp. Output	
7 (8)	V_{cc}		16 (19)	Electric Switch Input (2)	
8 (10)	FM Demod.	(1)	17 (21)	Differential Amp.	(1)
9 (11)	Capacitance	(2)	18 (22)	Input	(2)

In case of AN6328S, Pin No. ③, ⑨, ⑭, ⑳ are NC.

■ Application Circuit



□ shows the Pin No. of AN6328S

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