AN1324(AN6564), AN1324NS(AN6564NS)

Quadruple Operational Amplifiers

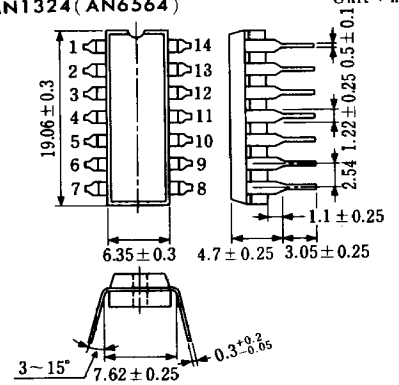
■ Outline

The AN1324 (AN6564) and the AN1324NS (AN6564NS) are quadruple operational amplifiers with phase compensation circuits built-in, and with wide range of operating voltages, allowing single power supply operation. They have electrical characteristics equal to the conventional operational amplifiers, and are low-powered and suited for application to various circuits.

■ Features

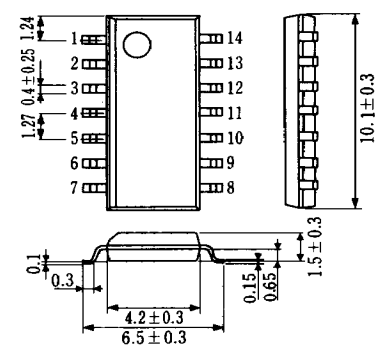
- Built-in phase compensation circuit
- Wide range of common-mode input voltage
  0V～Vcc－1.5V
- Wide range of operating voltages
  Single supply : 3～30V
  Dual supply : ±1.5～15V

AN1324(AN6564) Unit : mm



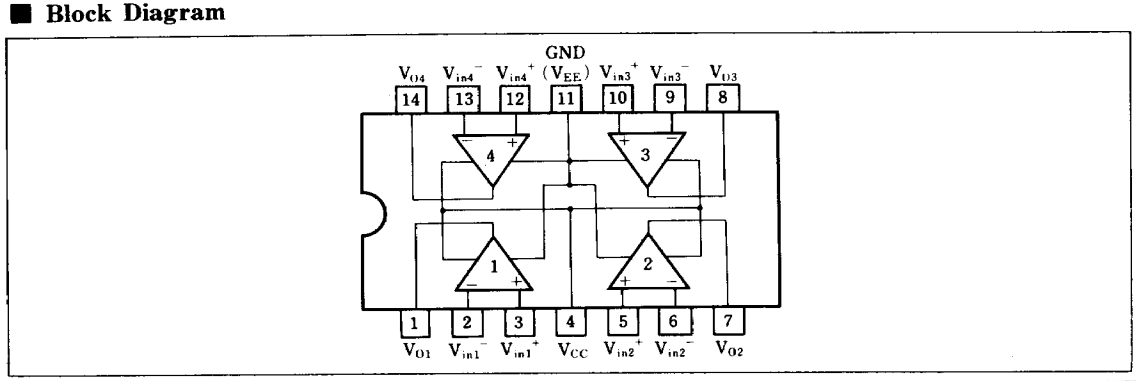
14-Lead DIL Plastic Package

AN1324NS(AN6564NS) Unit : mm



14-Lead PANAFLAT Package(SO-14D)

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Ch. 1 Output	8	Ch. 3 Output
2	Ch. 1 Invert Input	9	Ch. 3 Invert Input
3	Ch. 1 Non Invert Input	10	Ch. 3 Non Invert Input
4	Vcc	11	GND(V_{EE})
5	Ch. 2 Non Invert Input	12	Ch. 4 Non Invert Input
6	Ch. 2 Invert Input	13	Ch. 4 Invert Input
7	Ch. 2 Output	14	Ch. 4 Output

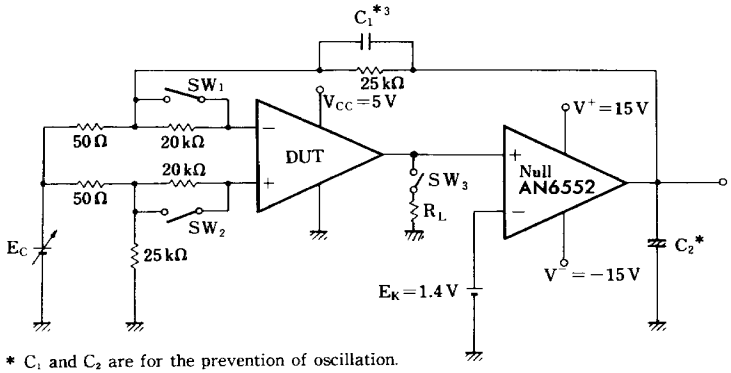
■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	32	V
	Differential Input Voltage	V_{ID}	32	V
	Common-Mode Input Voltage	V_{ICM}	−0.3~32	V
	Output Voltage	V_O	24	V
Power Dissipation	AN1324(AN6564)	P_D	570	mW
	AN1324NS(AN6564NS)		380	
Operating Ambient Temperature		T_{opr}	−20~+75	℃
Storage Temperature	AN1324(AN6564)	T_{stg}	−55~+150	℃
	AN1324NS(AN6564NS)		−55~+125	

■ Electrical Characteristics (V_{CC}=5V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	R_S=50Ω		2	7	mV
Input Bias Current	I_{Bias}	1				500	nA
Input Offset Current	I_{IO}	1				50	nA
Common-Mode Input Voltage Range	V_{CM}	2		0		Vcc−1.5	V
Supply Current	Icc	3	R_L=∞			2	mA
Voltage Gain	G_V	1	R_L≧2kΩ		100		dB
Maximum Output Voltage	$V_{O(max.)}$	4	R_L=2kΩ	Vcc−1.5			V
Common-Mode Rejection Ratio	CMR	1		65	85		dB
Supply Voltage Rejection Ratio	SVR	1		65	100		dB
Channel Separation	CS	5	f=1kHz~20kHz		120		dB
Output Source Current	$I_{O(source)}$	6	V_{in}^+=1V, V_{in}^-=0V	20	40		mA
Output Sink Current	I_{SINK}	7	V_{in}^+=0V, V_{in}^-=1V	10	20		mA

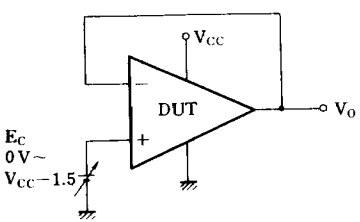
Test Circuit 1 ($V_{I(offset)}$, I_{Bias}, I_{IO}, G_V, CMR, SVR)



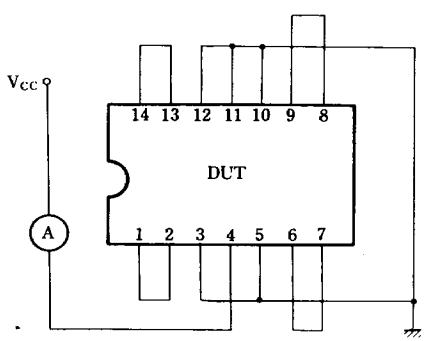
* C_1 and C_2 are for the prevention of oscillation.

Item	Measurement Conditions
Input Offset Voltage	V_{F1} is measured with both the SW_1 and SW_2 set to ON (SW_3 : OFF). Can be given by $V_{I(offset)}=\frac{V_{F1}}{500}$(V)
Input Offset Current	V_{F2} is measured with both the SW_1 and SW_2 set to OFF (SW_3 : OFF) . Can be given by $I_{IO}=\frac{\lvert V_{F2}-V_{F1}\rvert}{10^7}$(A)
Input Bias Current	V_{F3} is measured with the SW_1 set to ON and the SW_2 and SW_3 set to OFF. V_{F4} is measured with the SW_1 set to OFF and the SW_2 set to ON. Can be given by. $I_{Bias}=\frac{\lvert V_{F4}-V_{F3}\rvert}{2\times10^7}$(A)
Voltage Gain	V_{F5} is measured with the SW_1, SW_2 and SW_3 set to ON and $E_K=3.4V$ Can be given by $G_V=20\log\frac{1000}{\lvert V_{F1}-V_{F5}\rvert}$
Common-Mode Rejection Ratio	V_{F6} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF and $E_C=E_{C1}$. V_{F7} is measured with $E_C=E_{C2}$. Can be given by. $CMR=20\log\left(500\times\left\lvert\frac{E_{C1}-E_{C2}}{V_{F6}-V_{F7}}\right\rvert\right)$
Supply Voltage Rejection Ratio	V_{F8} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_C=0V$ and $V_{CC}=V_{C1}$. V_{F9} is measured with $V_{CC}=V_{C2}$. Can be given by. $SVR=20\log\left(500\times\left\lvert\frac{V_{C1}-V_{C2}}{V_{F8}-V_{F9}}\right\rvert\right)$

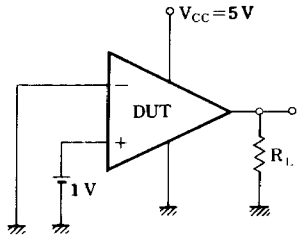
Test Circuit 2 (V_{CM})



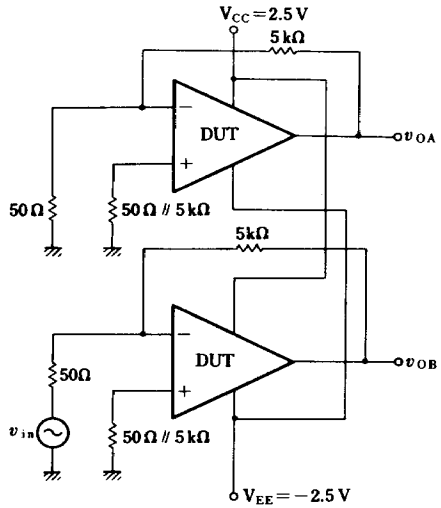
Test Circuit 3 (I_{CC})



Test Circuit 4 ($V_{O(max.)}$)

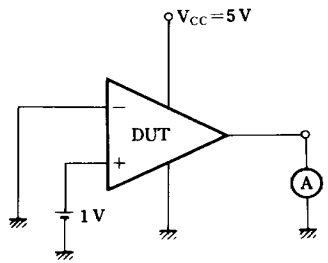


Test Circuit 5 (CS)

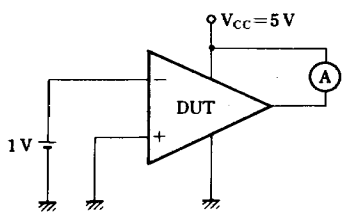


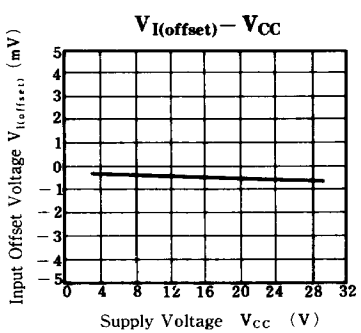
$$CS(B \rightarrow A) = 20 \log \left(100 \frac{v_{OB}}{v_{OA}} \right)$$

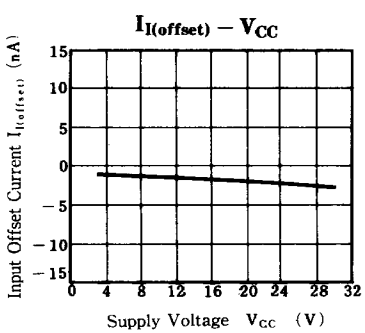
Test Circuit 6 ($I_{O(source)}$)

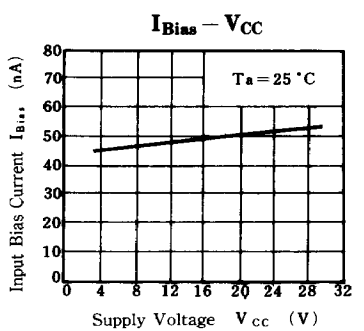


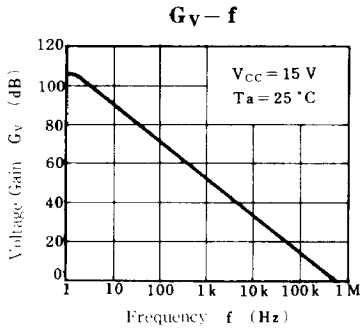
Test Circuit 7 (I_{SINK})

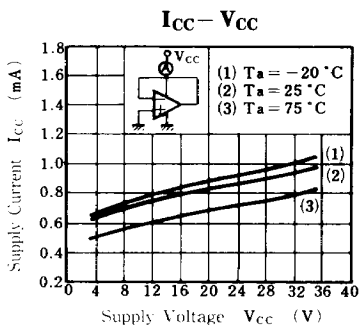


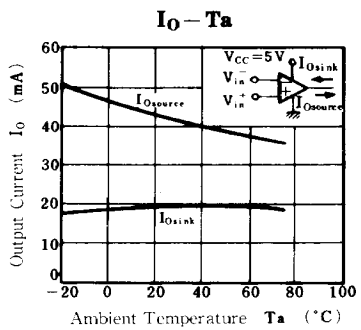


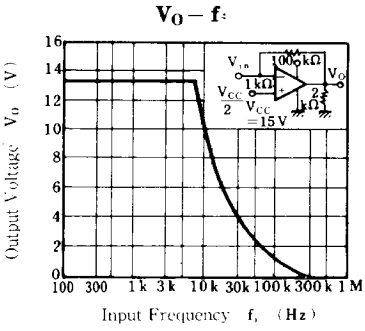


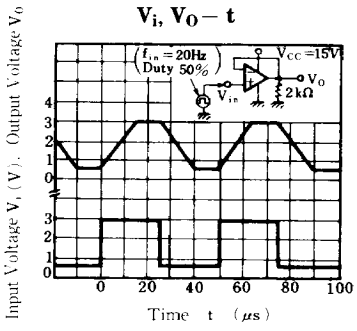


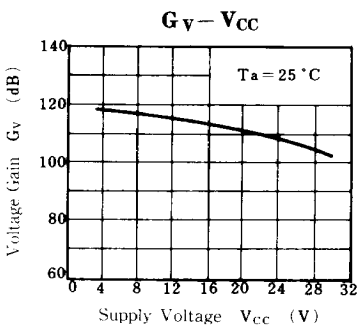












■ Application Circuit