

8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

6N137 Series

Features:

- High speed 10Mbit/s
- Fan out of 8 over -40 to 85°C
- Logic gate output
- High isolation voltage between input and output (Viso=5000 V rms)
- Compact small outline package
- Pb free and RoHS compliant.

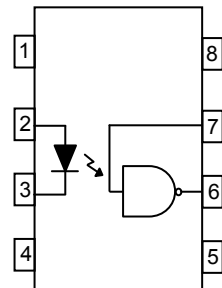


Description

The 6N137series devices each of consist of an infrared emitting diodes, optically coupled to a Very high speed integrated photo detector logic gate with a strobable output.

They are packaged in an 8-pin DIP package and available in wide-lead spacing and SMD option.

Schematic



Pin Configuration

- 1, 4. N.C
- 2, Anode
- 3, Cathode
- 5, Gnd
- 6, Vout
- 7, VE
- 8, VCC

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

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Absolute Maximum Ratings ($T_a=25^{\circ}\text{C}$)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	Enable input voltage Not exceed V_{CC} by more than 500mV	V_E	5.5	V
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	100	mW
Output	Power dissipation	P_C	85	mW
	Output current	I_O	50	mA
	Output voltage	V_O	7.0	V
	Supply voltage	V_{CC}	7.0	V
Output Power Dissipation		P_O	100	mW
Isolation voltage ^{*1}		V_{ISO}	5000	V rms
Operating temperature		T_{OPR}	-55 ~ +85	$^{\circ}\text{C}$
Storage temperature		T_{STG}	-55 ~ +125	$^{\circ}\text{C}$
Soldering temperature ^{*2}		T_{SOL}	260	$^{\circ}\text{C}$

Notes

*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 & 2 are shorted together, and pins 3 & 4 are shorted together.

*2 For 10 seconds.

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Electrical Characteristics ($T_a = -40$ to 85°C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	$I_F = 10\text{mA}$
Reverse voltage	V_R	5.0	-	-	V	$I_R = 10\mu\text{A}$
Input capacitance	C_{IN}	-	60	-	pF	$V_F=0, f=1\text{MHz}$

Output

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
High level supply current	I_{CCH}	-	7	10	mA	$I_F=10\text{mA}, V_E=0.5\text{V}, V_{CC}=5.5\text{V}$
Low level supply current	I_{CCL}	-	9	13	mA	$I_F=0\text{mA}, V_E=0.5\text{V}, V_{CC}=5.5\text{V}$
High level enable current	I_{EH}	-	-0.6	-1.6	mA	$V_E=0.5\text{V}, V_{CC}=5.5\text{V}$
Low level enable current	I_{EL}	-	-0.8	-1.6	mA	$V_E=2.0\text{V}, V_{CC}=5.5\text{V}$
High level enable voltage	V_{EH}	2.0	-	-	V	$I_F=10\text{mA}, V_{CC}=5.5\text{V}$
Low level enable voltage	V_{EL}	-	-	0.8	V	$I_F=10\text{mA}, V_{CC}=5.5\text{V}$

Transfer Characteristics ($T_a = -40$ to 85°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
High Level Output Current	I_{OH}	-	-	100	μA	$V_{CC}=5.5\text{V}, V_O=5.5\text{V}, I_F=250\mu\text{A}, V_E=2.0\text{V}$
Low Level Output Current	V_{OL}	-	0.35	0.6	V	$V_{CC}=5.5\text{V}, I_{CL}=13\text{mA}, I_F=5\text{mA}, V_E=2.0\text{V}$
Input Threshold Current	I_{FT}	-	2.5	5	mA	$V_{CC}=5.5\text{V}, V_O=0.6\text{V}, V_E=2.0\text{V}, I_{OL}=13\text{mA}$

* Typical values at $T_a = 25^\circ\text{C}$

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Switching Characteristics ($T_a = -40$ to 85°C , $V_{CC} = 5\text{V}$, $I_F = 7.5\text{mA}$ unless specified otherwise)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Propagation delay time to output High level	T_{PHL}	-	35	75	μS	$C_L = 15\text{pF}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$
Propagation delay time to output Low level	T_{PLH}	-	40	75	μS	$C_L = 15\text{pF}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$
Pulse width distortion	$T_{PHL} - T_{PLH}$	-	-	35	ns	$C_L = 15\text{pF}$, $R_L = 350\Omega$
Output rise time	t_r	-	40	50	ns	$C_L = 15\text{pF}$, $R_L = 350\Omega$
Output full time	t_f	-	10	30	ns	$C_L = 15\text{pF}$, $R_L = 350\Omega$
Enable Propagation Delay Time to Output High Level	t_{ELH}	-	15	-	ns	$I_F = 7.5\text{mA}$, $V_{EH} = 3.5\text{V}$, $C_L = 15\text{pF}$, $R_L = 350\Omega$
Enable Propagation Delay Time to Output Low Level	t_{EHL}	-	15	-	ns	$I_F = 7.5\text{mA}$, $V_{EH} = 3.5\text{V}$, $C_L = 15\text{pF}$, $R_L = 350\Omega$
Common Mode Transient Immunity at Logic High	CM_H	5000	-	-	$\text{V}/\mu\text{S}$	$I_F = 0\text{mA}$, $V_{CM} = 50\text{Vp-p}$, $V_{OH} = 2.0\text{V}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$
Common Mode Transient Immunity at Logic Low	CM_L	5000	-	-	$\text{V}/\mu\text{S}$	$I_F = 7.5\text{mA}$, $V_{CM} = 50\text{Vp-p}$, $V_{OL} = 0.8\text{V}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$

* Typical values at $T_a = 25^\circ\text{C}$

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Typical Performance Curves

Fig.1 Input Diode Forward Voltage vs. Forward Current

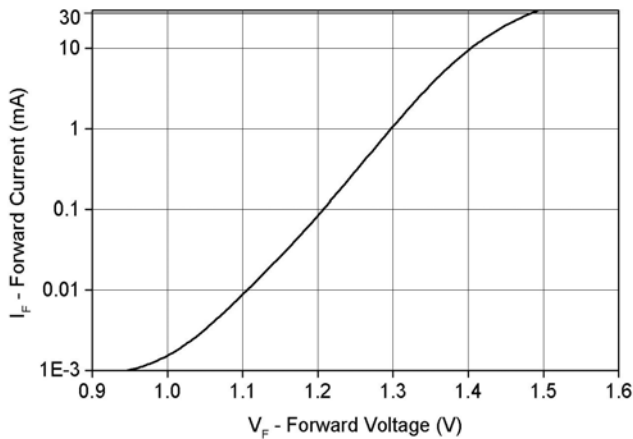


Fig.2 Low Level Output Voltage vs. Ambient Temperature

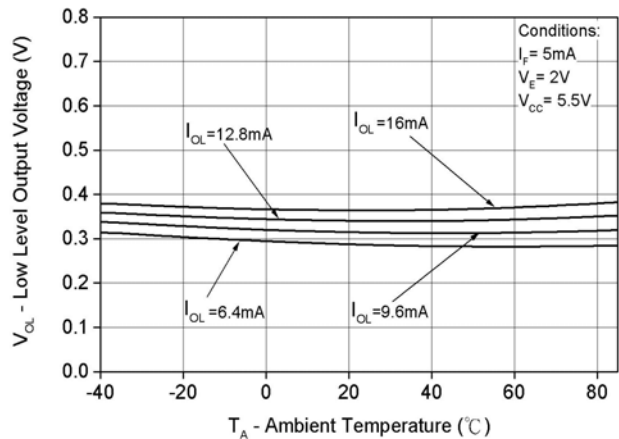


Fig.3 Low Level Output Current vs. Ambient Temperature

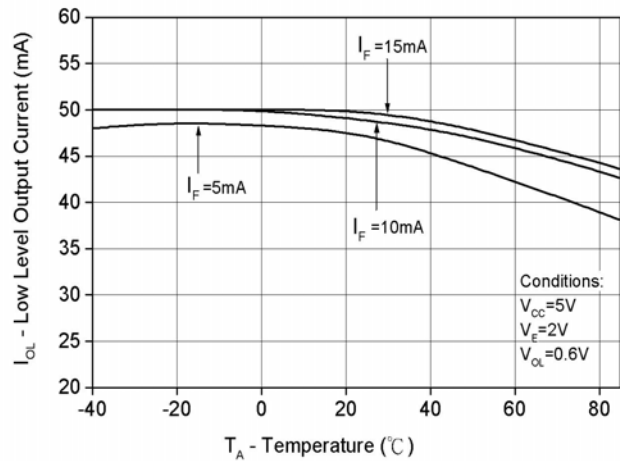
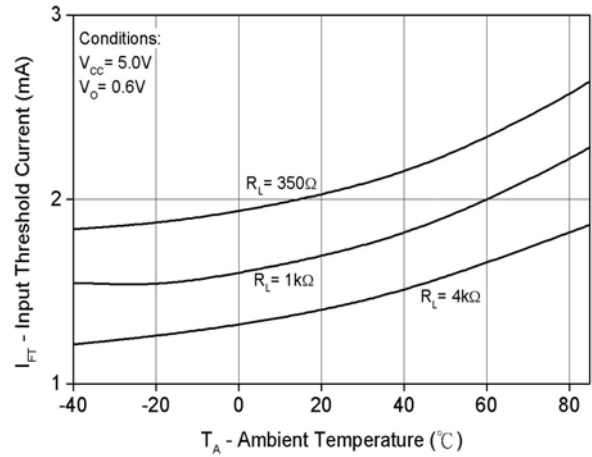


Fig.4 Input Threshold Current vs. Ambient Temperature



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Fig.5 Output Voltage vs. Input Forward Current

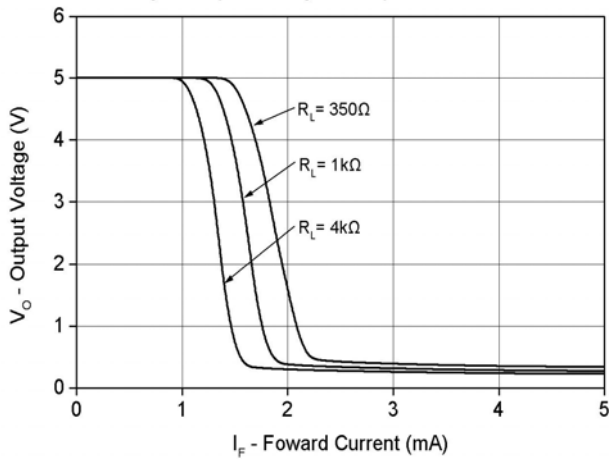


Fig.6 High Level Output Current vs. Temperature

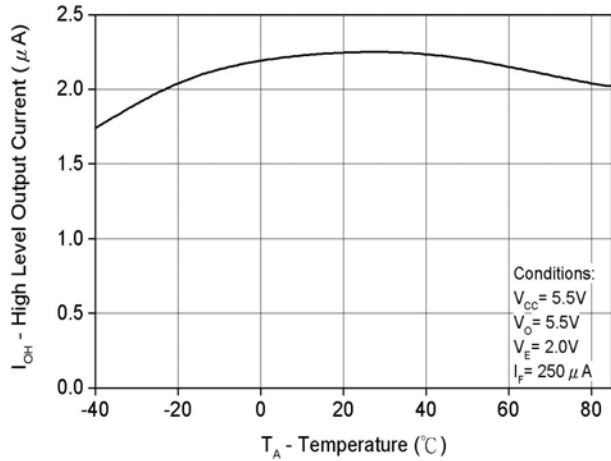


Fig.7 Switching Time vs. Forward Current

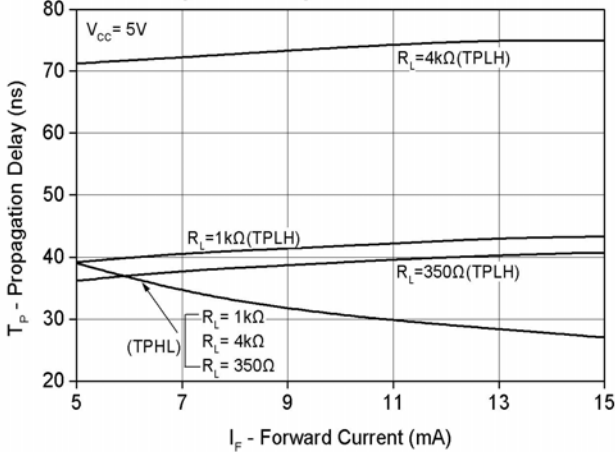


Fig.8 Switching Time vs. Temperature

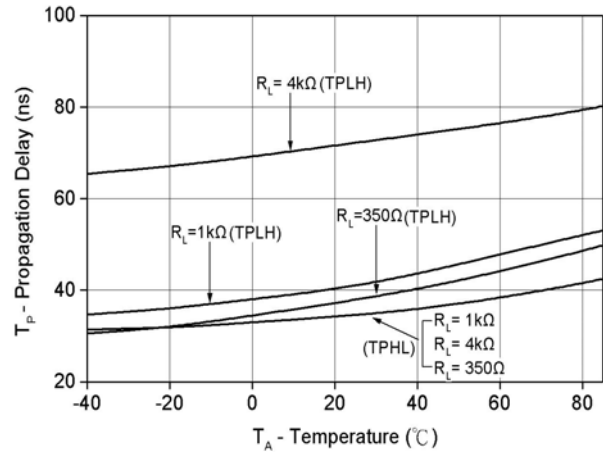


Fig.9 Pulse Width Distortion vs. Temperature

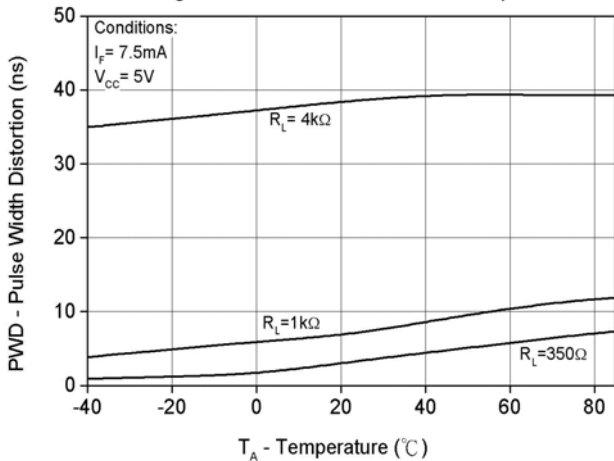
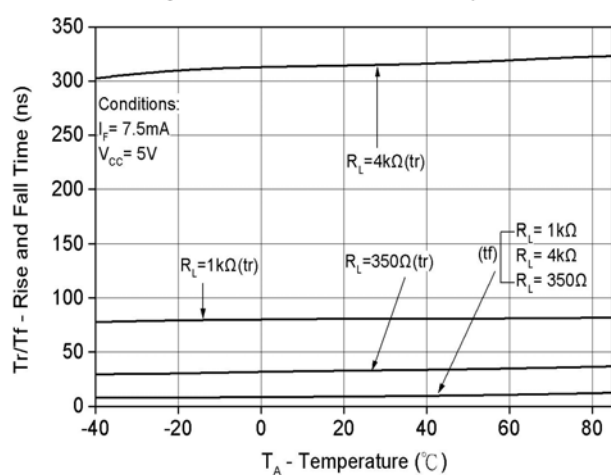


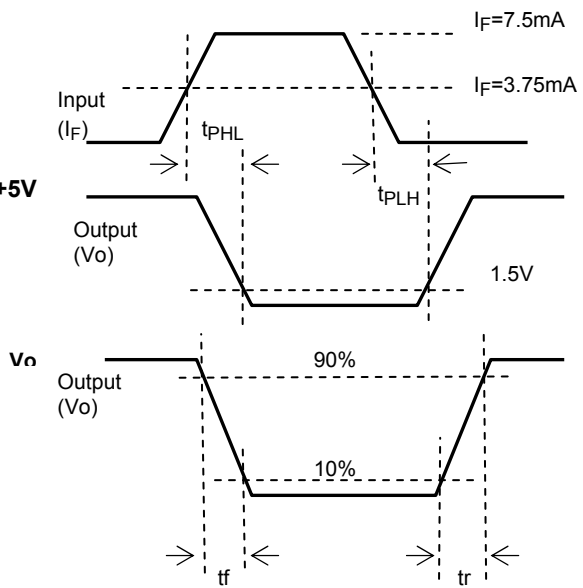
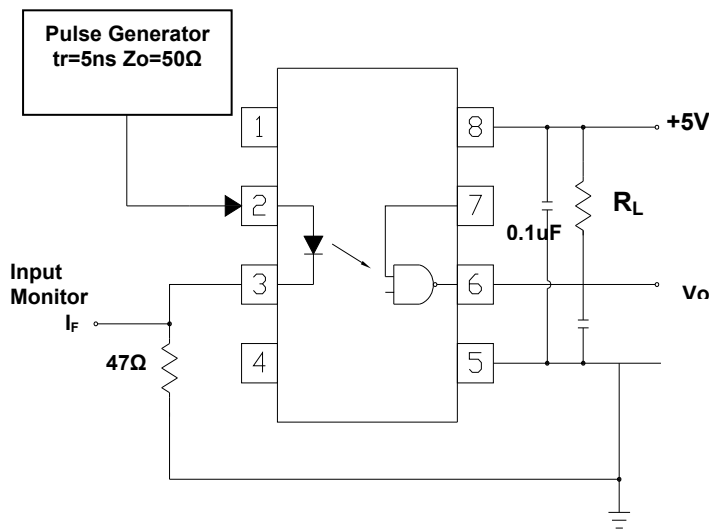
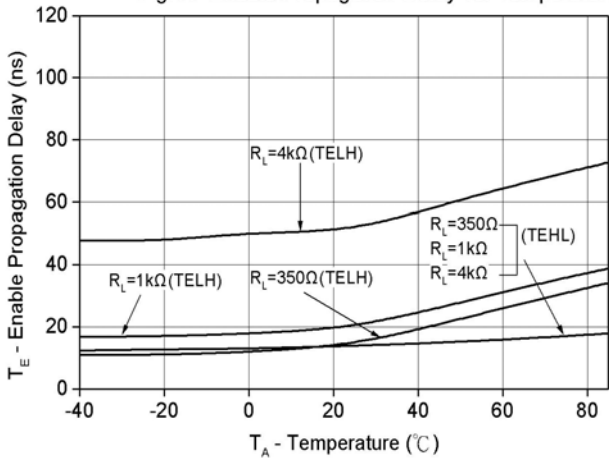
Fig.10 Rise and Fall Time vs. Temperature



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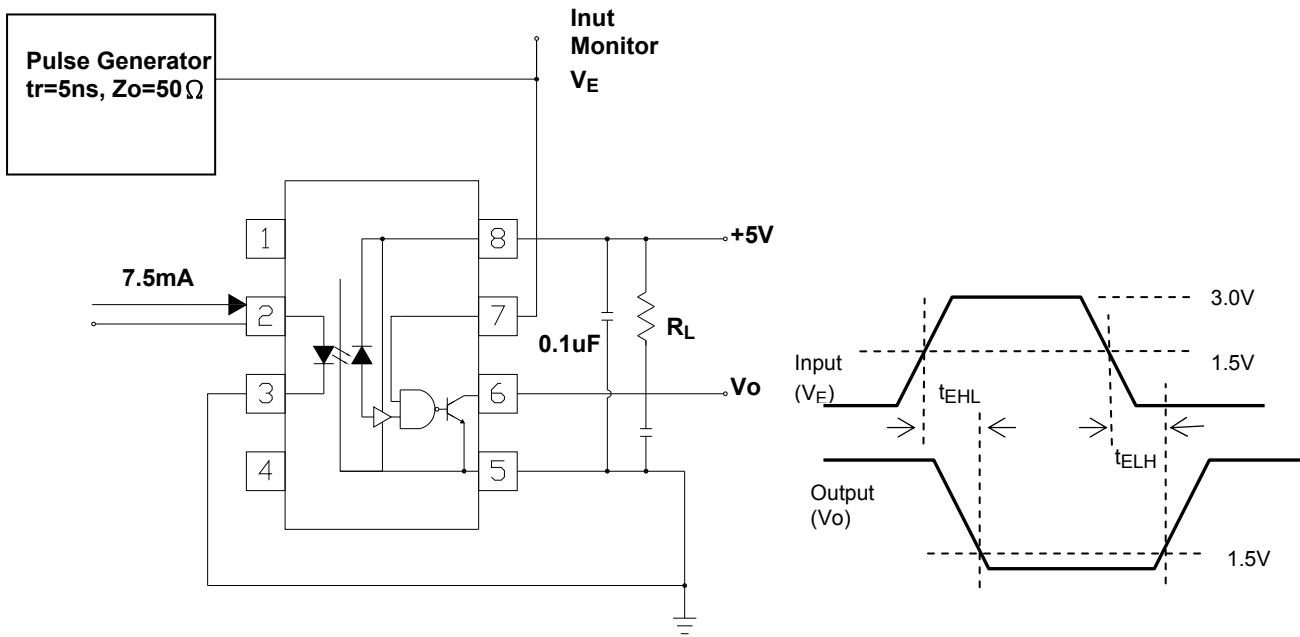
Fig.11 Enable Propagation Delay vs. Temperature



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Fig. 12 Test circuit and waveforms for t_{PHL} , t_{PLH} , t_r , and t_f



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Fig. 13 Test circuit for t_{EHL} and t_{ELH}

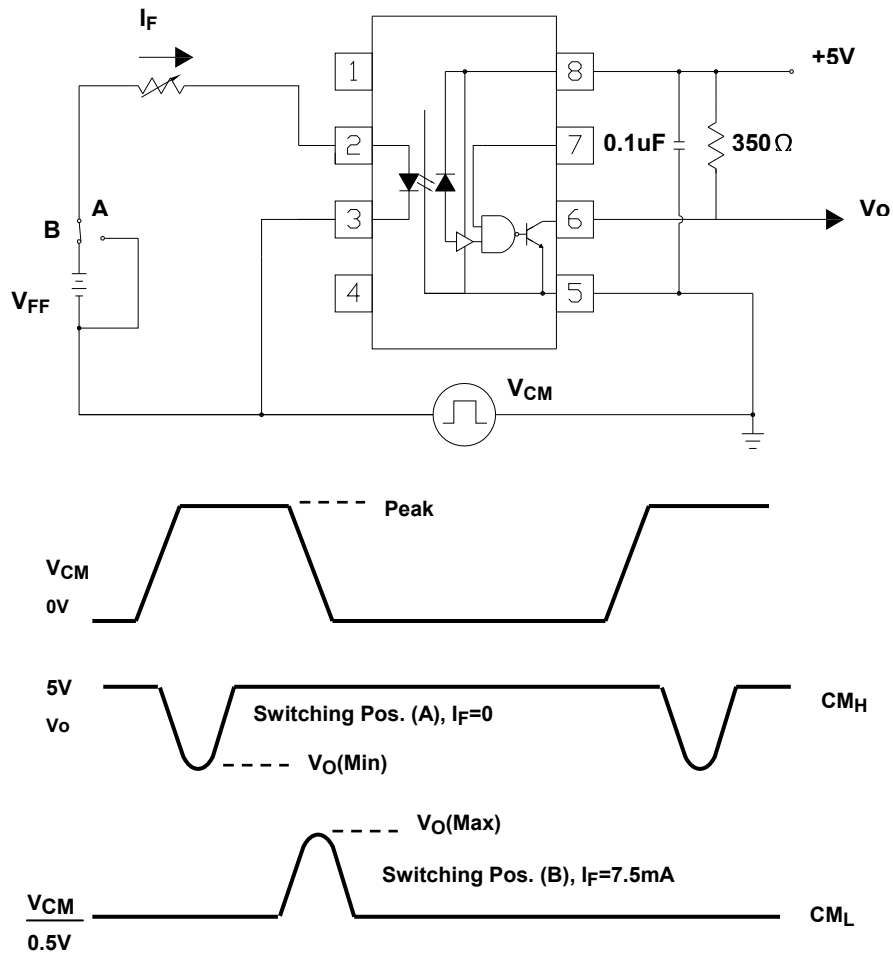
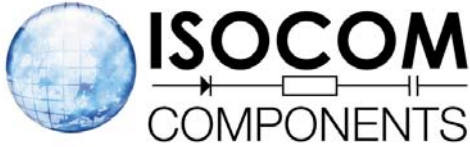


Fig. 14 Test circuit Common mode Transient Immunity



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Order Information

Part Number

6N137Y

Note

Y = Lead form option (G SM SM T+R or none)

Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
G	Wide lead bend (0.4 inch spacing)	45 units per tube
SM	Surface mount lead form	45 units per tube
SM T+R	Surface mount lead form + tape & reel option	1000 units per reel

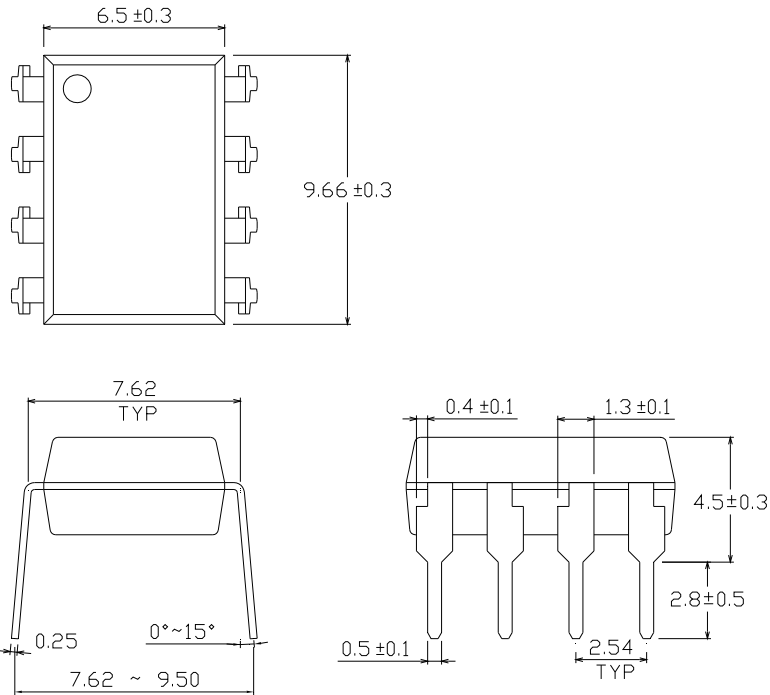
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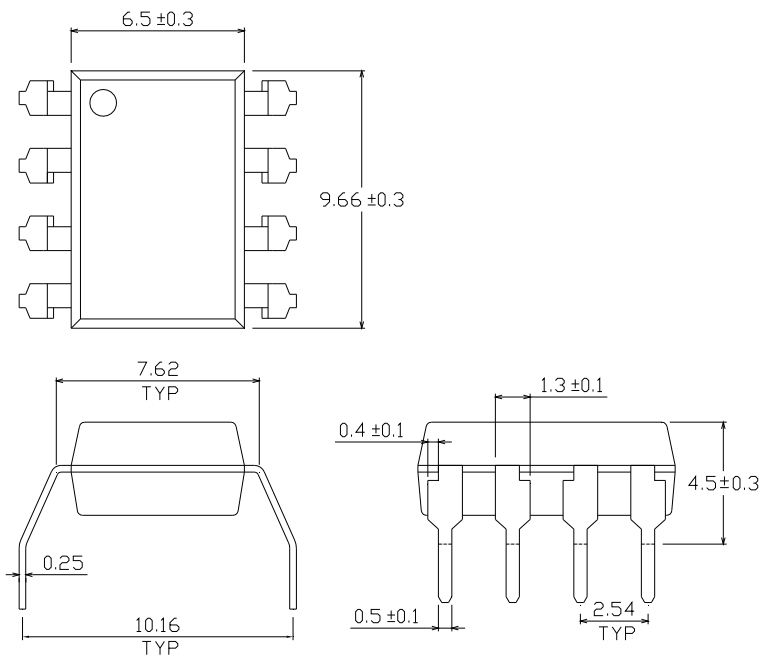
Package Drawing

(Dimensions in mm)

Standard DIP Type



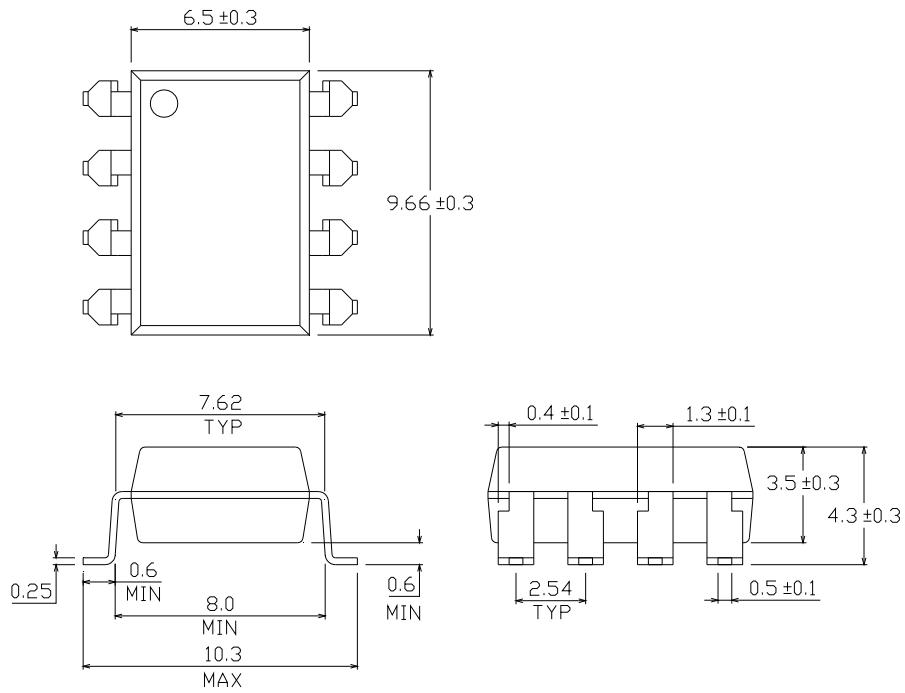
Option G Type



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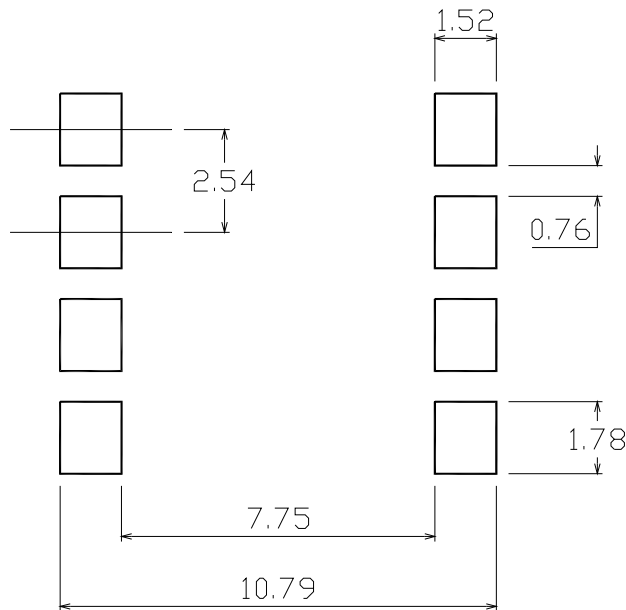
Option SM Type



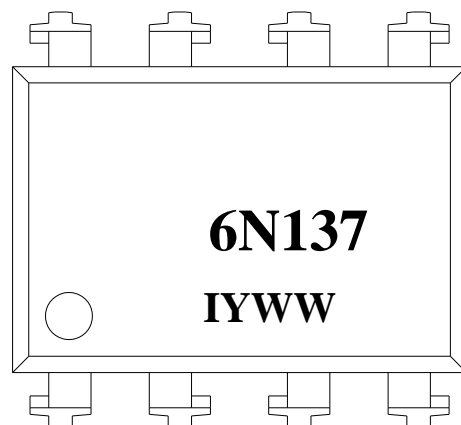
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Recommended pad layout for surface mount leadform



Device Marking



Notes

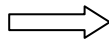
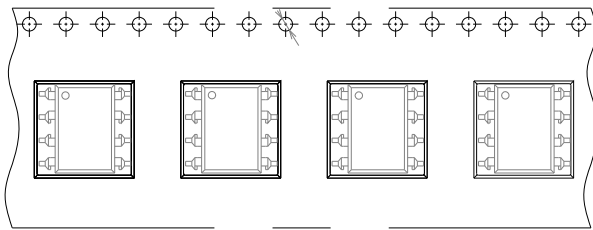
- 6N137 denotes Device Number
- Y denotes 1 digit Year code
- WW denotes 2 digit Week code
- I denotes Isocom

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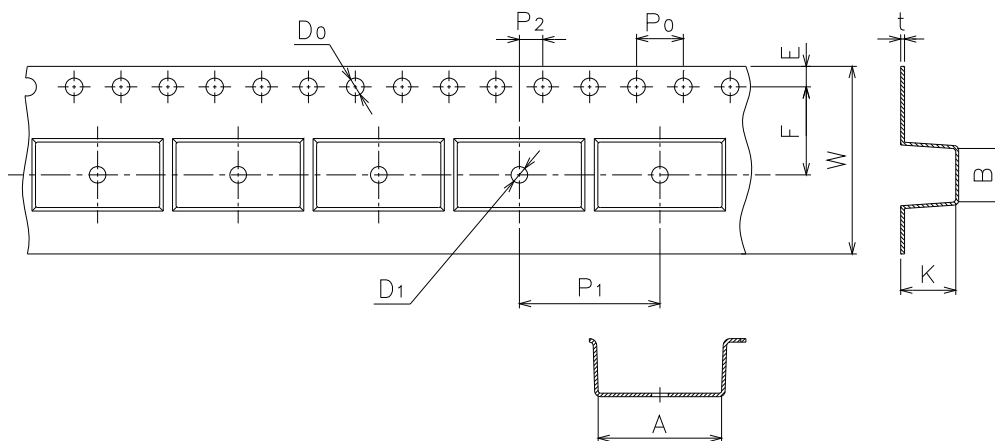
Tape & Reel Packing Specifications

Option T+R



Direction of feed from reel

Tape dimensions

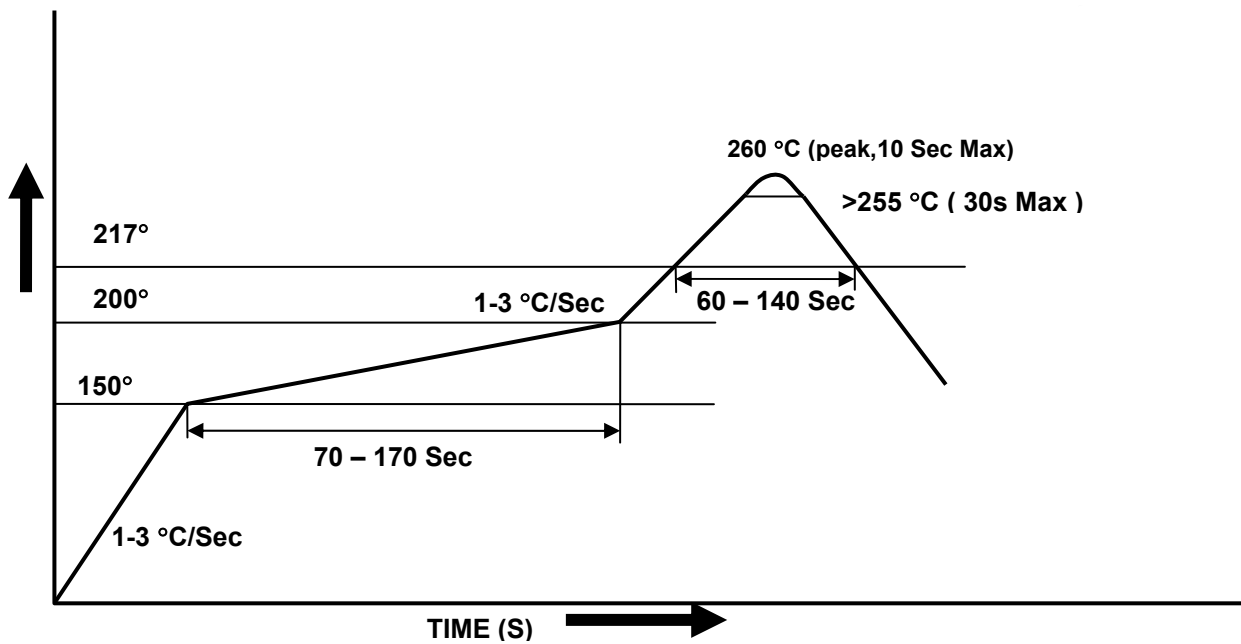


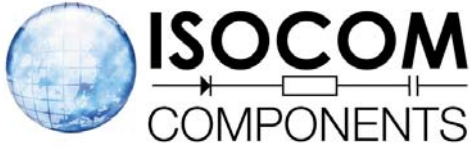
Dimension No.	A	B	Do	D1	E	F
Dimension(mm)	10.4±0.1	10.0±0.1	1.5±0.1	1.5±0.1	1.75±0.1	7.5±0.1
Dimension No.	Po	P1	P2	t	W	K
Dimension(mm)	4.0±0.1	12.0±0.1	2.0±0.1	0.4±0.1	16.0+0.3/ -0.1	4.5±0.1

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Solder Reflow Temperature Profile





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