

# AN3313, AN3313S

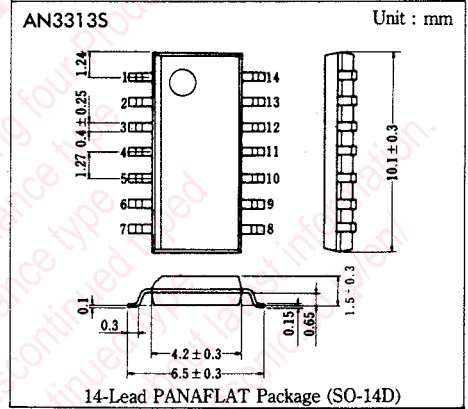
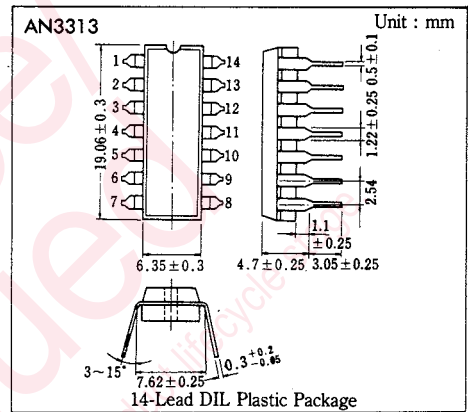
## Head Amplifier Circuits for VTR (2-Head Type)

### ■ Outline

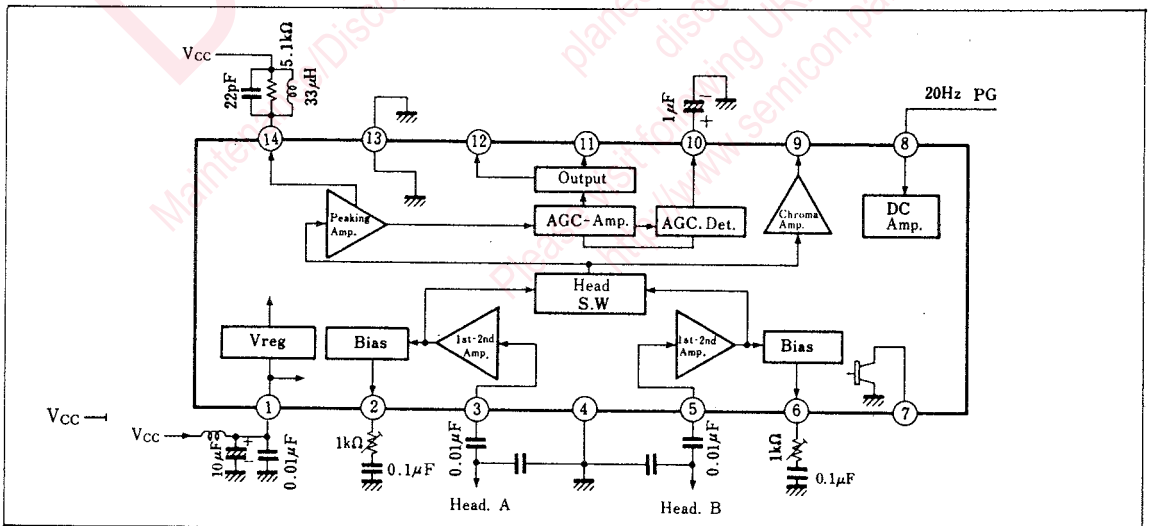
The AN3313 and the AN3313S are integrated circuits designed for head amplifier circuits for VTR (2-head type).

### ■ Features

- Supply voltage :  $V_{CC}=5V$
- Built-in peaking amplifier circuit
- Less noise voltage to input ( $1\mu V_{rms}$ )



### ■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>CC</sub>	8	PG Pulse Input
2	CH1 Damping Adjustment	9	Chroma Signal Output
3	CH1 Input	10	AGC Level Detection
4	GND	11	AGC Output B
5	CH2 Input	12	AGC Output A
6	CH2 Damping Adjustment	13	GND
7	ON Switch at PB	14	Peaking

■ Absolute Maximum Ratings (T<sub>a</sub>=25°C)

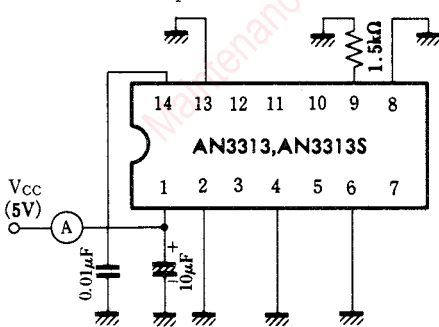
Item	Symbol	Rating	Unit
Supply Voltage	V <sub>CC</sub>	6.0	V
Power Dissipation (T <sub>a</sub> =70°C)	P <sub>D</sub>	130	mW
Operating Ambient Temperature	T <sub>opr</sub>	-20~+70	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

■ Electrical Characteristics (V<sub>CC</sub>=5V, T<sub>a</sub>=25°C)

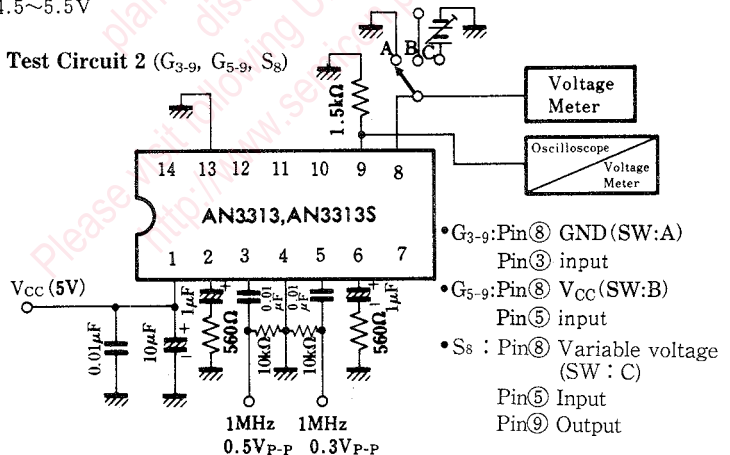
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I <sub>1</sub>	1	②, ⑥, ⑩ GND. ④ 1.5×Ω GND. ⑭ V <sub>CC</sub>	10		24	mA
Ch1 Gain	G <sub>3-9</sub>	2	③ 1MHz, 0.5mV <sub>P-P</sub> . ⑨ Out	52.5		62.5	dB
Ch2 Gain	G <sub>5-9</sub>	2	⑤ 1MHz, 0.5mV <sub>P-P</sub> . ⑨ Out	52.5		62.5	dB
AGC Output Amplitude	v <sub>12</sub>	3	③ 4MHz, 0.3mV <sub>P-P</sub> . ⑫ Out	154		286	mV <sub>P-P</sub>
AGC Control Sensitivity	Δv <sub>12</sub>	3	③ 4MHz, 0.3mV <sub>P-P</sub> . ⑫ Out			3	dB
PG Switch Changeover Sensitivity	S <sub>8</sub>	2	③ 1MHz, 0.5mV <sub>P-P</sub> . ⑥ GND ⑧ Variable voltage ⑨ out			3.5	V
Noise Voltage Referred to Input(1)	V <sub>ni1</sub>	4	⑥ GND ⑨ Out 1MHz BPF added			1	μV <sub>rms</sub>
Noise Voltage Referred to Input(2)	V <sub>ni2</sub>	4	⑧ V <sub>CC</sub> ⑨ Out 1MHz BPF added			1	μV <sub>rms</sub>

Note : Operating supply voltage range V<sub>CC(oper)</sub>=4.5~5.5V

Test Circuit 1 (I<sub>1</sub>)



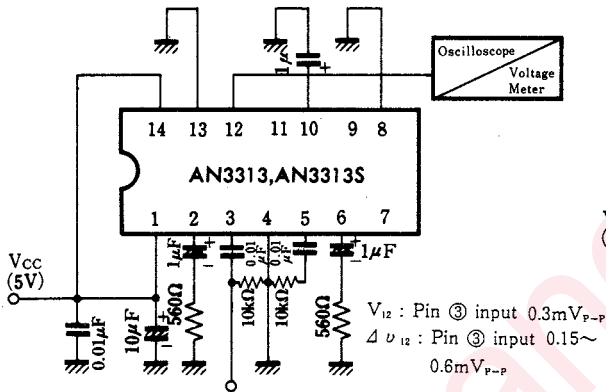
Test Circuit 2 (G<sub>3-9</sub>, G<sub>5-9</sub>, S<sub>8</sub>)



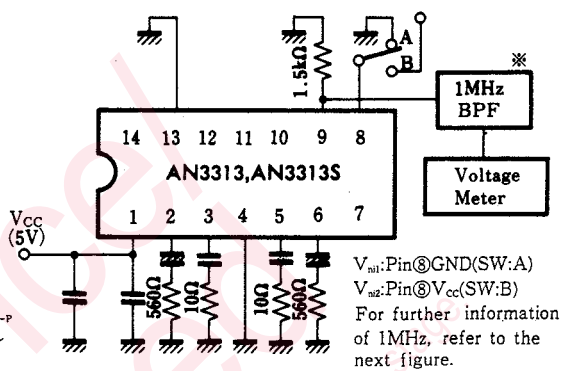
- G<sub>3-9</sub>: Pin ⑧ GND (SW:A)  
Pin ③ input
- G<sub>5-9</sub>: Pin ⑧ V<sub>CC</sub> (SW:B)  
Pin ⑤ input
- S<sub>8</sub> : Pin ⑧ Variable voltage (SW:C)  
Pin ⑤ Input  
Pin ⑨ Output

Increasing the electric potential of Pin ⑧ from 0V, measure the electric potential of Pin ⑧ when Pin ⑨ output appears.

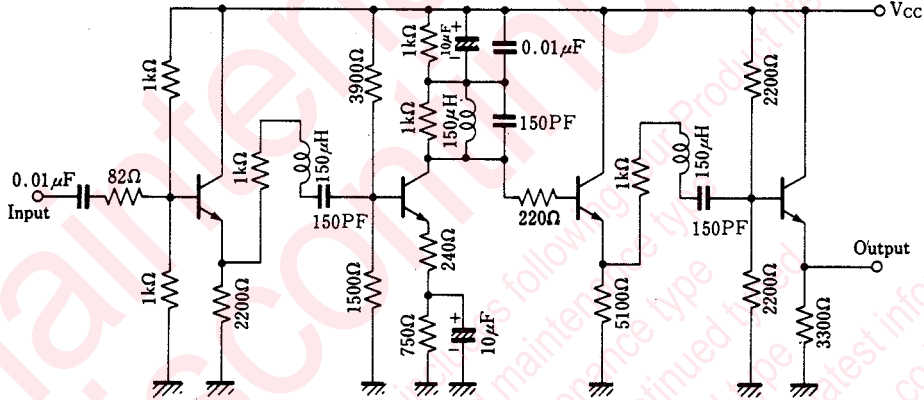
Test Circuit 3 ( $v_{i2}$ ,  $\Delta v_{i2}$ )



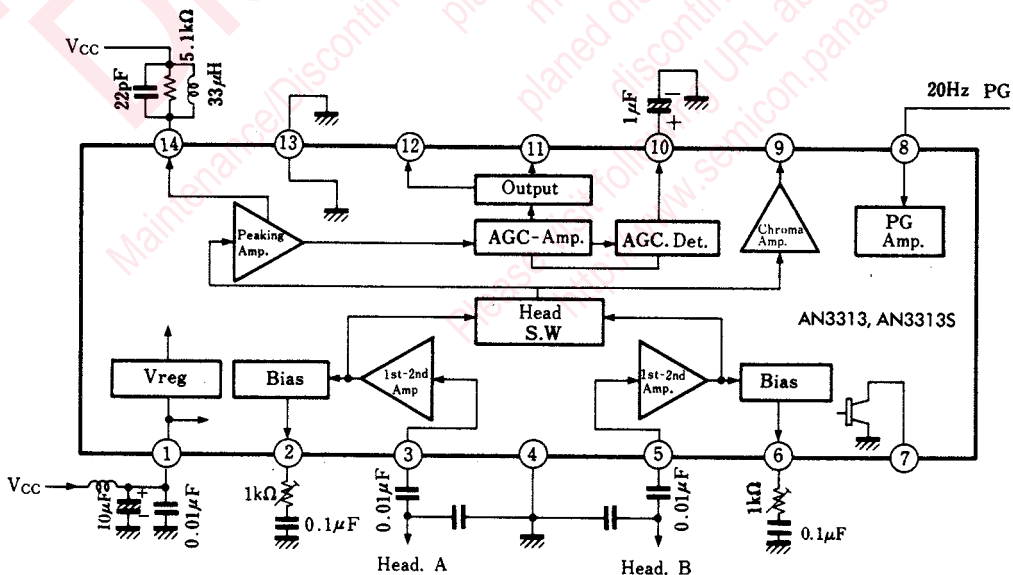
Test Circuit 4 ( $V_{ni1}$ ,  $V_{ni2}$ )



\* 1MHz BPF



■ Application Circuit



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