
HA13150A

21 W × 4-Channel BTL Power IC

HITACHI

ADE-207-107
1st. Edition

Description

HA13150A is a four-channel BTL amplifier IC designed for car audio, featuring high output and low distortion, and applicable to digital audio equipment. It provides 21 W output per channel, with a 14.4 V power supply and at 10% distortion.

Functions

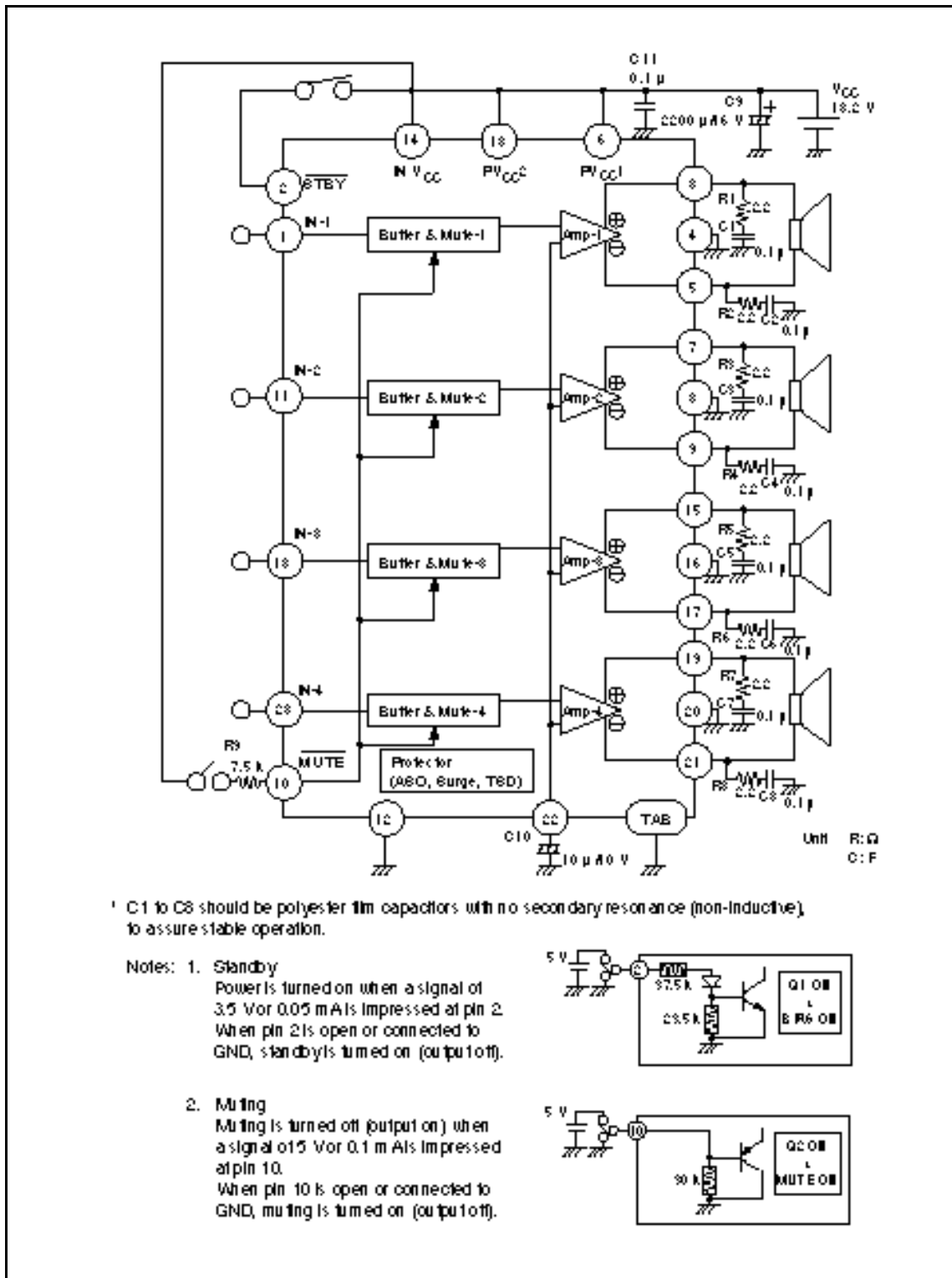
- Built-in standby circuit
- Built-in muting circuit
- Built-in protection circuits (surge, TSD, and ASO)

Features

- Requires few external parts
- Low distortion (total harmonic distortion = 0.01% at 3 W)
- Low noise (at $R_g = 620 \Omega$, noise is 0.15 mV (muting off) or 0.1 mV (muting on))
- Popping noise minimized
- Highly reliable current-limiting ASO protector keeps speakers safe from all kinds of trouble. Reliability is further enhanced by a fast-acting thermal shutdown protection circuit with on/off hysteresis.

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Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

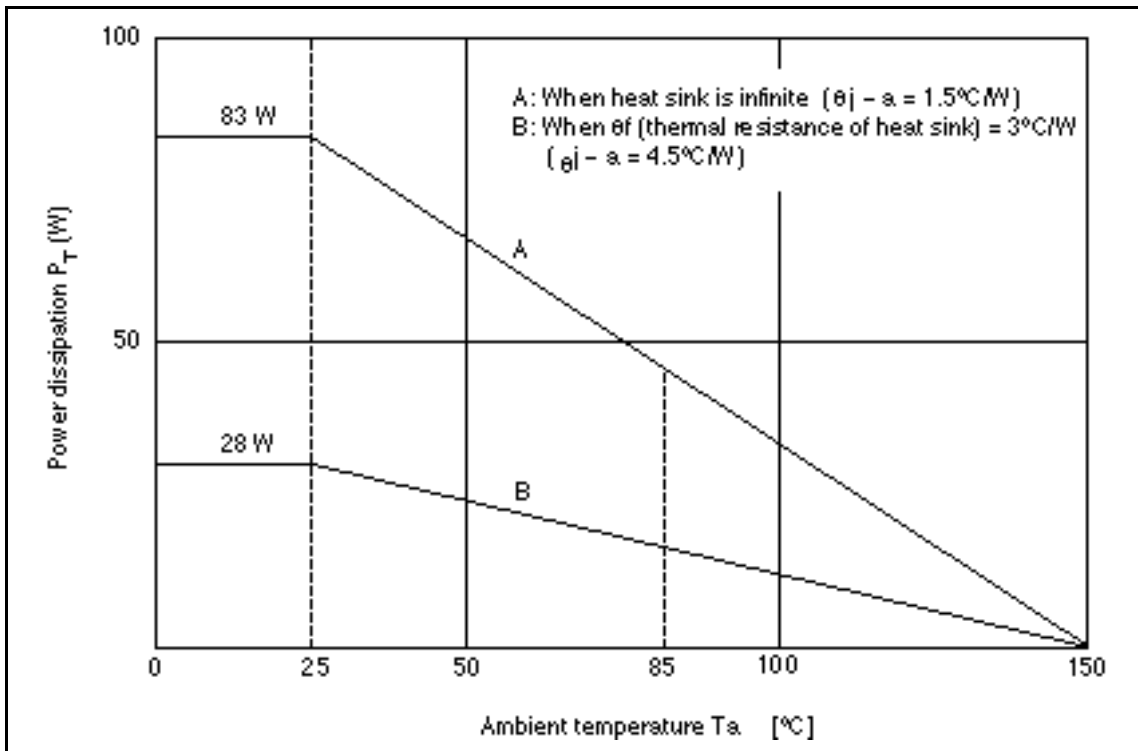
Item	Symbol	Rating	Unit	Remarks
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Operating supply voltage	V_{CC}	18	V
Supply voltage when no signal ^{*1}	V_{CC} (DC)	26	V
Peak supply voltage ^{*2}	V_{CC} (PEAK)	50	V
Output current ^{*3}	I_O (PEAK)	4	A
Power dissipation ^{*4}	P_T	83	W
Junction temperature	T_j	150	°C
Operating temperature	T_{opr}	-30 to +85	°C
Storage temperature	T_{stg}	-55 to +125	°C

- Notes: 1. Tolerance within 30 seconds
 2. Tolerance in surge pulse waveform
 3. Value per 1 channel
 4. Value when attached on the infinite heat sink plate at $T_a = 25^\circ\text{C}$.
 The derating curve is as shown in the graph below.

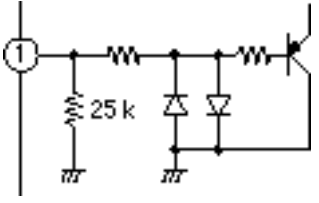
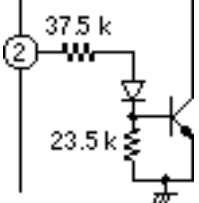
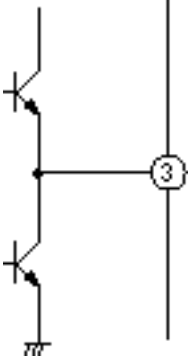
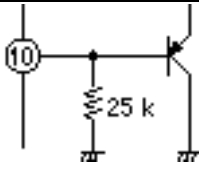


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Electrical Characteristics ($V_{CC} = 13.2 \text{ V}$, $f = 1 \text{ kHz}$, $R_L = 4 \text{ } \Omega$, $R_g = 620 \text{ } \Omega$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Current when no signal	Iq1	—	240	—	mA	Vin = 0
Output offset voltage	Vq	-250	0	+250	mV	
Gain	Gv	30.5	32	33.5	dB	
Gain difference between channels	Gv	-1.5	0	+1.5	dB	
Rated output power	Po	—	18	—	W	$V_{CC} = 13.2 \text{ V}$ $R_L = 4 \text{ } \Omega$, THD = 10%
Max output power	Pomax	—	30	—		$V_{CC} = 13.7 \text{ V}$ $R_L = 4 \text{ } \Omega$, THD = Max
Total harmonic distortion	T.H.D	—	0.01	—	%	Po = 3 W
Output noise voltage	WBN	—	0.15	0.5	mVrms	Rg = 0 BW = 20 to 20 kHz
Ripple rejection	SVR	—	55	—	dB	Rg = 600 f = 120 Hz
Channel crosstalk	C.T	—	70	—	dB	Rg = 600 Vout = 0 dBm
Input impedance	Rin	—	25	—	k	
Standby current	Iq2	—	—	200	μA	
Standby control voltage (high)	V _{STH}	3.5	—	V _{CC}	V	
Standby control voltage (low)	V _{STL}	0	—	1.5	V	
Muting control voltage (high)	V _{MH}	3.5	—	V _{CC}	V	
Muting control voltage (low)	V _{ML}	0	—	1.5	V	
Muting attenuation	A _{TTM}	—	70	—	dB	Vout = 0 dBm

Pin Explanation

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
1	IN1	CH1 INPUT	25 k (Typ)	0 V	
11	IN2	CH2 INPUT			
13	IN3	CH3 INPUT			
23	IN4	CH4 INPUT			
2	STBY	Standby control	90 k (at Trs. cutoff)	—	
3	OUT1 (+)	CH1 OUTPUT	—	$V_{cc}/2$	
5	OUT1 (-)				
7	OUT2 (+)	CH2 OUTPUT			
9	OUT2 (-)				
15	OUT3 (+)	CH3 OUTPUT			
17	OUT3 (-)				
19	OUT4 (+)	CH4 OUTPUT			
21	OUT4 (-)				
10	MUTE	Muting control	25 k (Typ)	—	

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Pin Explanation (cont)

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
22	RIPPLE	Bias stability	—	$V_{CC}/2$	
6	PV_{CC1}	Power of output stage	—	V_{CC}	—
18	PV_{CC2}				
14	INV_{CC}	Power of input stage	—	V_{CC}	—
4	CH1 GND	CH1 power GND	—	—	—
8	CH2 GND	CH2 power GND			
16	CH3 GND	CH3 power GND			
20	CH4 GND	CH4 power GND			
12	IN GND	Input signal GND	—	—	—

Point of Application Board Design

1. Notes on Application board's pattern design
 - For increasing stability, the connected line of V_{CC} and OUTGND is better to be made wider and lower impedance.
 - For increasing stability, it is better to place the capacitor between V_{CC} and GND ($0.1 \mu\text{F}$) close to IC.
 - For increasing stability, it is better to place C1 to C8 and R1 to R8, which are for stopping oscillation, close to IC.
 - It is better to place the grounding of resistor (R_g), between input line and ground, close to INGND (Pin 12) because if OUTGND is connected to the line between R_g and INGND, THD will become worse due to current from OUTGND.

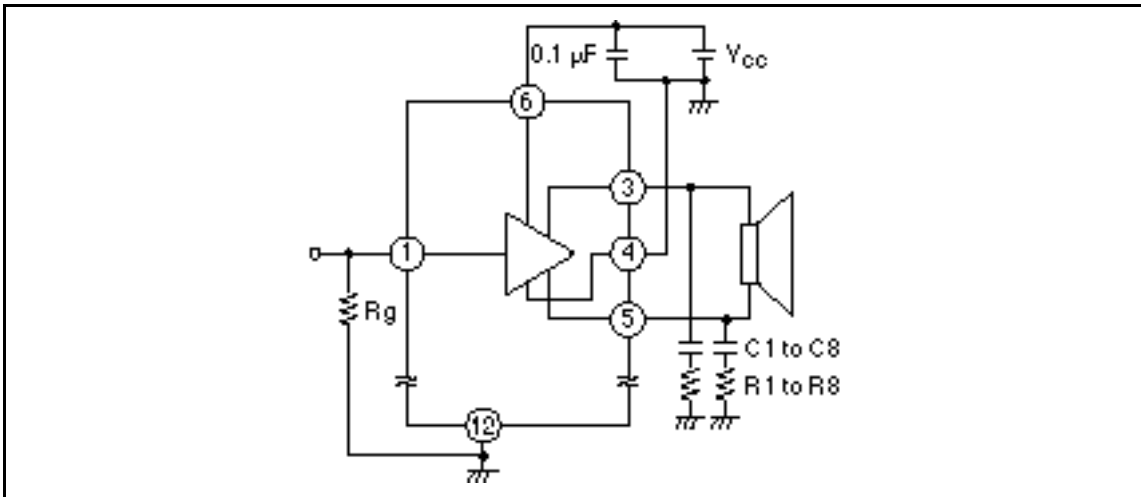


Figure 1 Notes on Application Board's Pattern Design

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2. How to reduce the popping noise by Muting circuit

At normal operating circuit, Muting circuit operates at high speed under 1 μ s.

In case popping noise becomes a problem, it is possible to reduce the popping noise by connecting capacitor, which determines the switching time constant, between pin 10 and GND. (Following figure 2)

We recommend value of capacitor greater than 1 μ F.

Also transitional popping noise can be reduced sharply by muting before V_{CC} and Standby are ON/OFF.

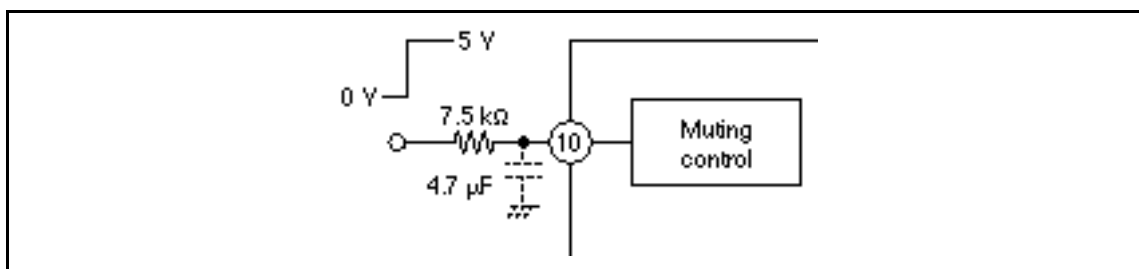
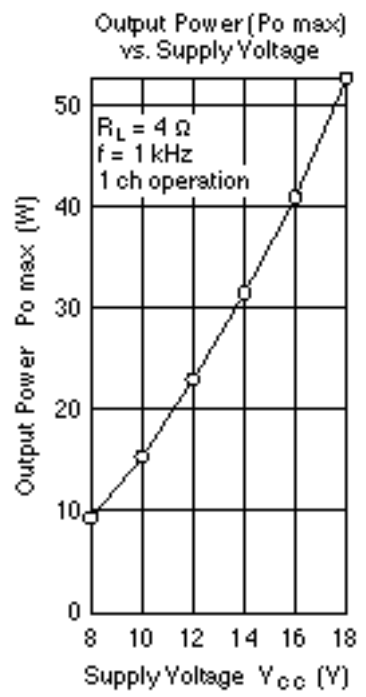
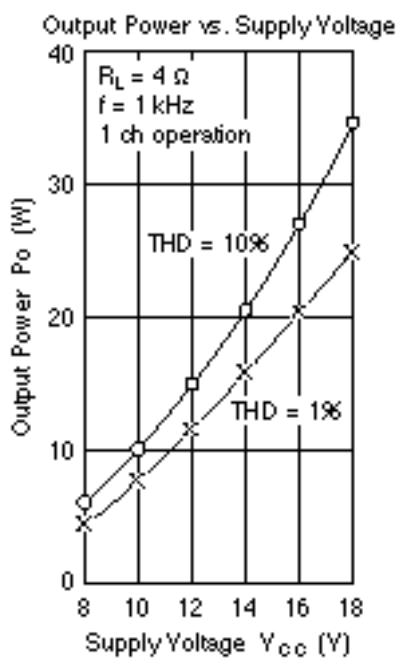
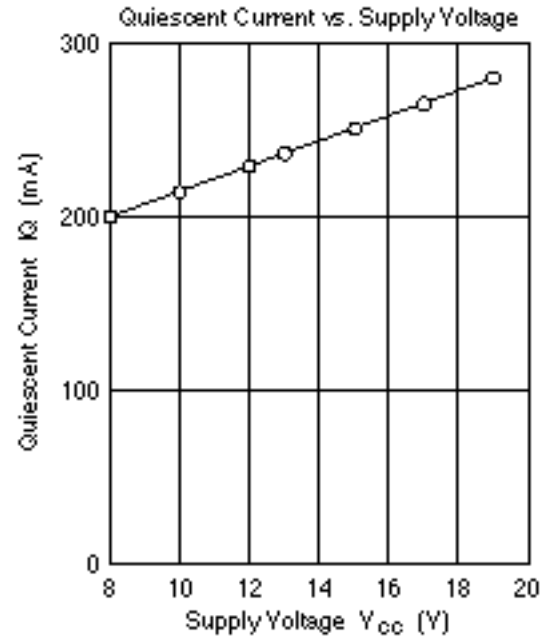
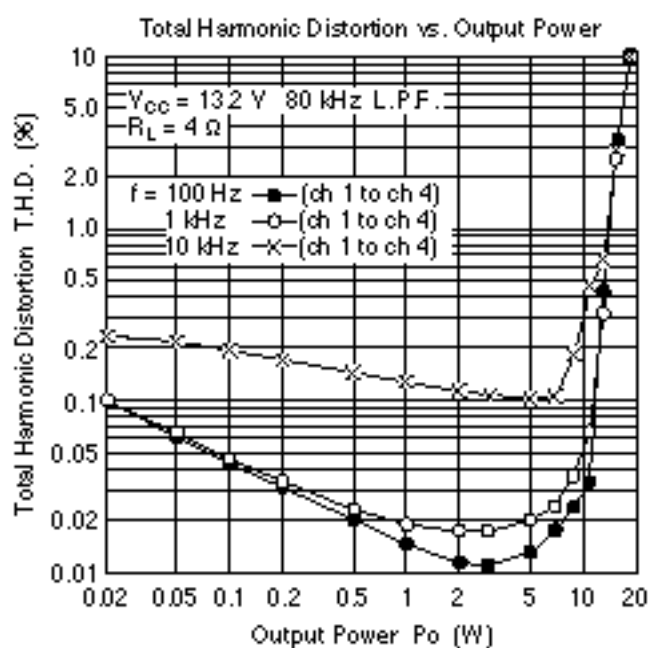
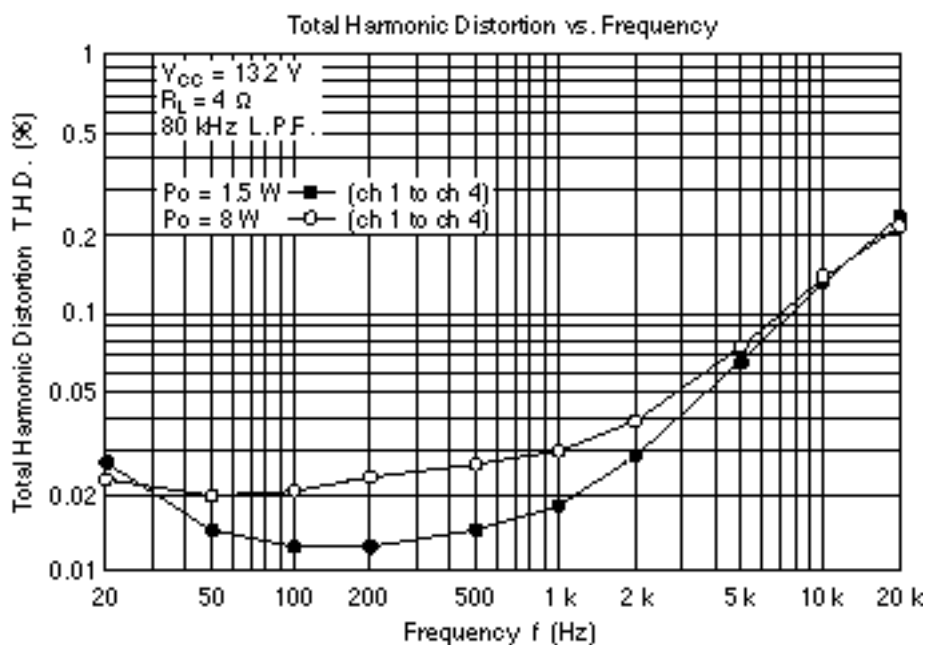


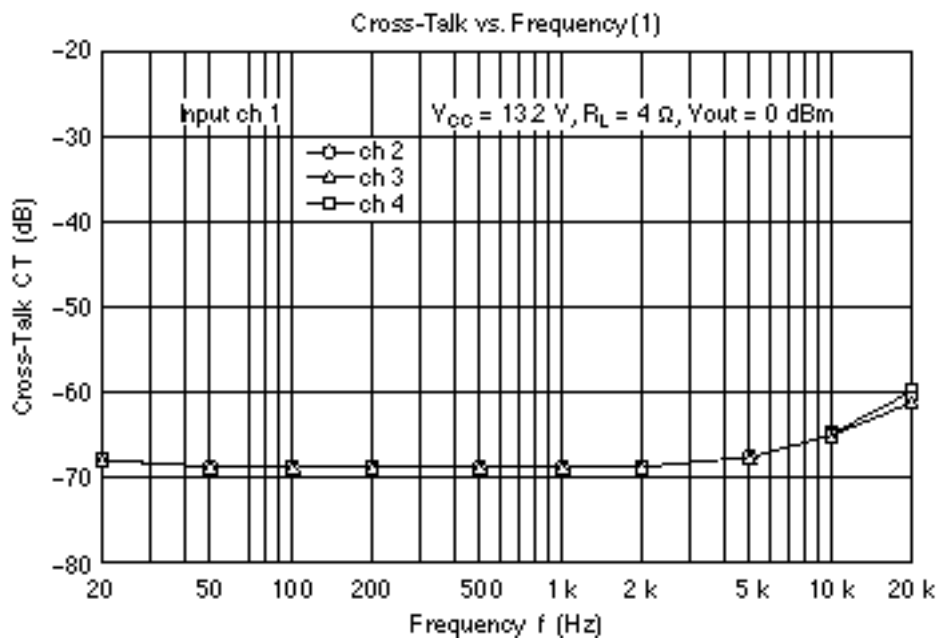
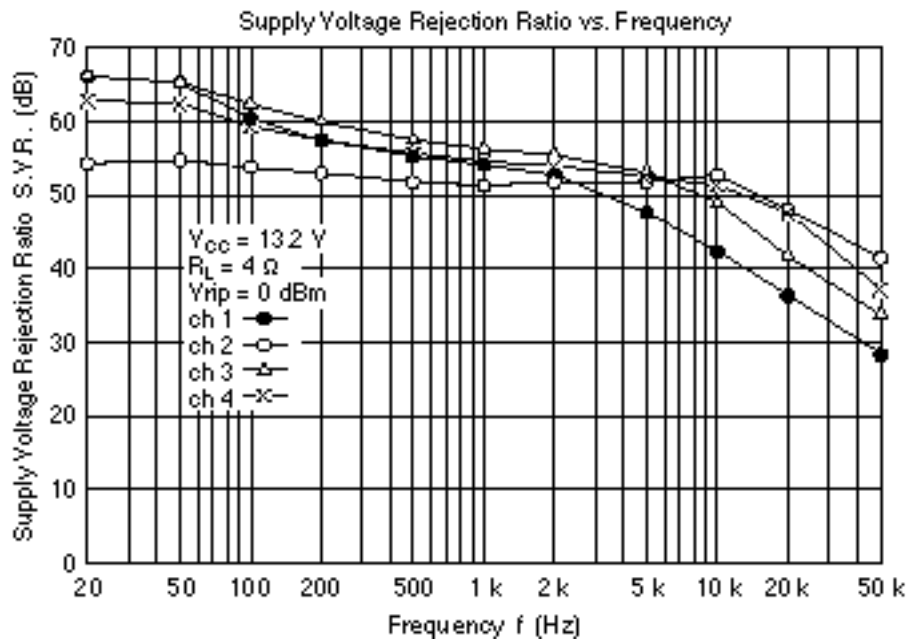
Figure 2 How to use Muting Circuit

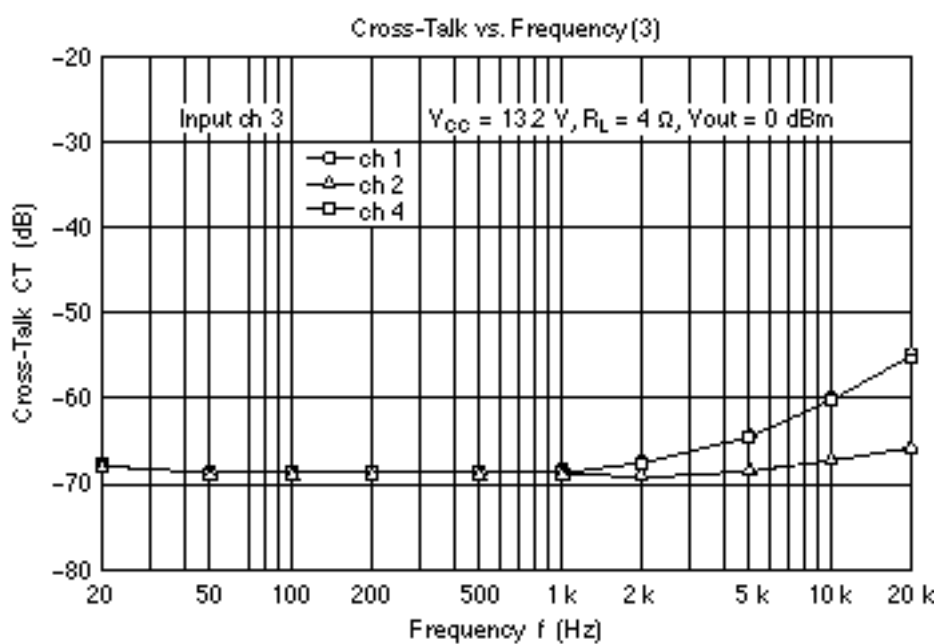
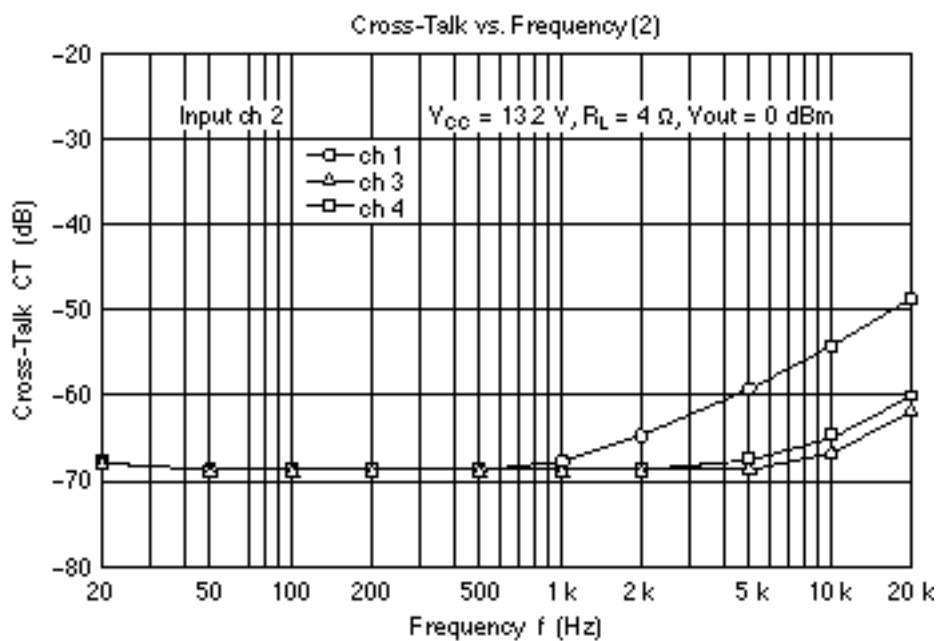
Table 1 Muting ON/OFF Time

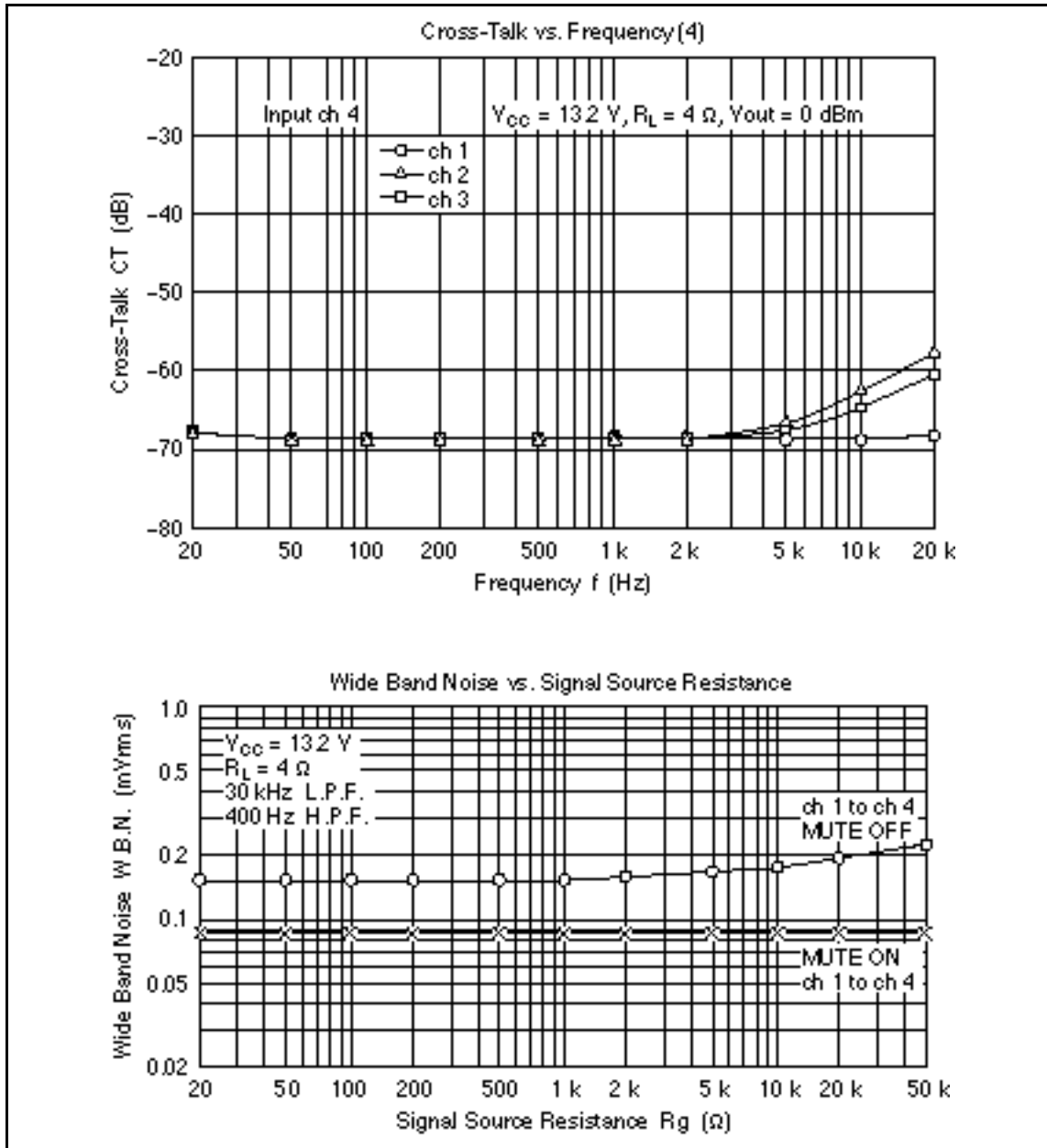
C (μ F)	ON Time	OFF Time
nothing	under 1 μ s	under 1 μ s
0.47	2 ms	2 ms
4.7	19 ms	19 ms



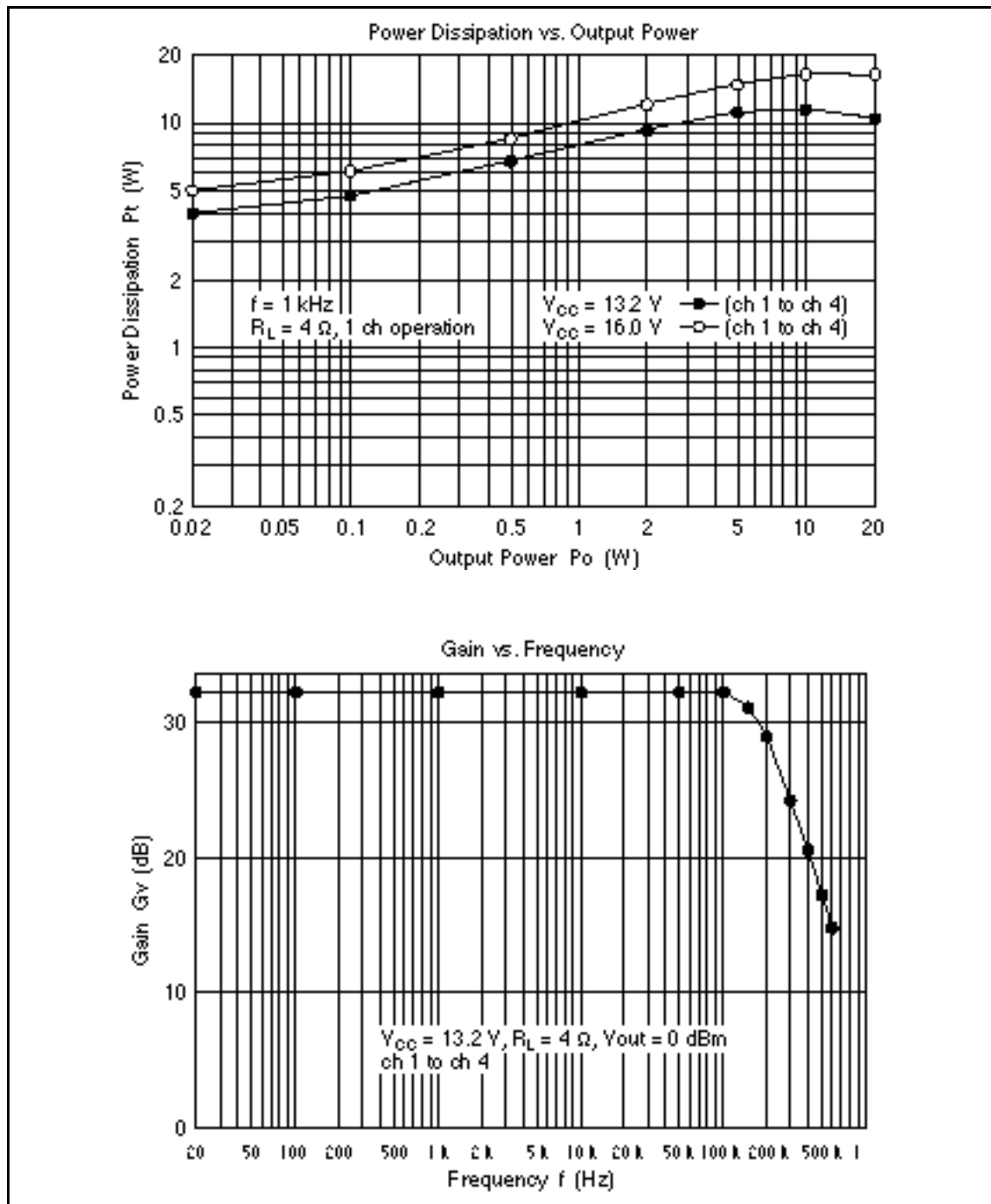








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