Ordering number: EN2260D

SANYO

No. 2260D

LC6527C/H, 6528C/H

CMOS LSI

SINGLE-CHIP 4-BIT MICROCOMPUTERS FOR SMALL-SCALE CONTROL-ORIENTED APPLICATIONS

General Description

The LC6527C/H, LC6528C/H are single-chip 4-bit microcomputers fabricated using CMOS process technology and are suited for use in small-scale control-oriented applications. The LC6527C/H, LC6528C/H are placed in 18-pin plastic packages.

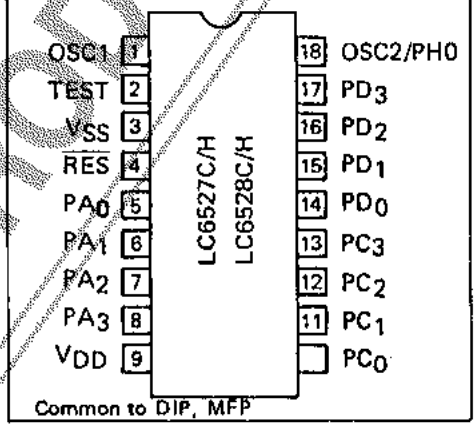
The LC6527 and LC6528 differ from each other as follows:

Type No.	ROM Capacity	RAM Capacity
LC6527C/H	1024 bytes	64 words
LC6528C/H	512 bytes	32 words

The H version (high speed version) and C version (wide operating voltage version) differ from each other as follows:

Type No.	Cycle Time	Operating Voltage
LC6527H LC6528H	0.92 to 20μsec	4.5 to 6.0V
LC6527C	6.0 to 20μsec	3.0 to 6.0V
LC6528C	2.77 ~ 20μsec	4.0 to 6.0V

Pin Assignment



Common to DIP, MFP

Features

(1) High speed operation 0.92μsec. cycle time
H version (LC6527H, LC6528H)

(2) Wide operating voltage range 3.0 to 6.0V
C version (at 6.0μsec. cycle time)

(3) Low power dissipation mode
Standby function provided by HALT instruction execution

(4) High current drive, LED drivable
I_{OL}: 10mA typ., 20mA max.

(5) High breakdown voltage input/output 15V max.

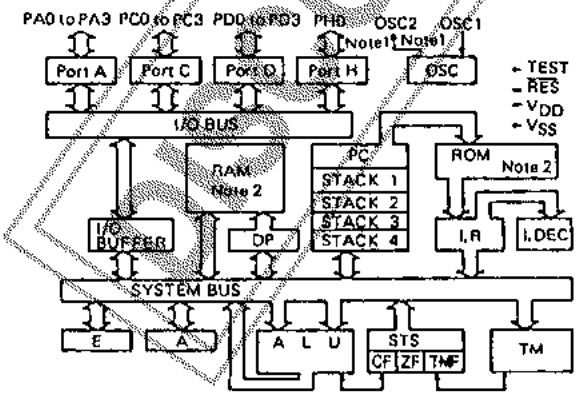
(6) 8-bit programmable timer
With 4-bit prescaler, overflow flag

(7) 4-level subroutine nesting

(8) Wide clock frequency range
200kHz to 4.33MHz (with 1/1, 1/3, 1/4 clock prescaler option)

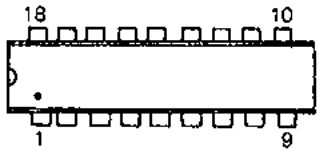
(9) 18-pin plastic package (DIP, MFP)

LC6527C/H, LC6528C/H System Block Diagram



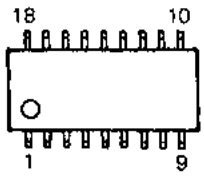
Package

i) DIP18



Note 3

ii) MFP18



Note 1 Either PH0 or OSC2 is selected by mask option.

Note 2 Differs with Type Nos. LC6527C/H: ROM 1024 bytes, RAM 64 words
LC6528C/H: ROM 512 bytes, RAM 32 words

Note 3 When mounting the MFP version on the board, do not dip it in solder.

Specifications and information herein are subject to change without notice.

SANYO Electric Co.,Ltd. Semiconductor Overseas Marketing Div.
Natsume Bldg., 18-6, 2-chome, Yushima Bunkyo-ku, TOKYO 113 JAPAN

Development Support

The following are available to support the LC6527, LC6528 program development.

(1) User's Manual

"LC6527, LC6528 User's Manual" No. E24.

(Note) Do not use "LC6523 Series User's Manual" No. E16.

(2) Development Tool Manual

For the EVA-410 system, refer to the description of Development Support Tools in "LC6527, LC6528 User's Manual". For the EVA-800 system, refer to "EVA800-LC6527/28 Development Tool Manual"

(3) Development Tools

1) For program development (EVA-410 system)
   - i. (SDS-410) system
   - ii. CP/M80 base cross assembler: (LC6527. COM), (LC6528. COM)
     MS-DOS base cross assembler: (LC6527C. COM), (LC6527H. COM), (LC6528C. COM), (LC6528H. COM)
   - iii. Evaluation kit (EVA-410C)
   - iv. Evaluation kit target board (EVA-TB6523C/26C/27C/28C), evaluation chip (LC6596)

2) For program evaluation
   - i. Piggyback (LC65PG23/26)
   - ii. Socket for conversion of number of piggyback pins (23T27)

Note. For notes for program evaluation, do not fail to refer to "4-3. Notes on Evaluation" in "LC6527, LC6528 User's Manual".

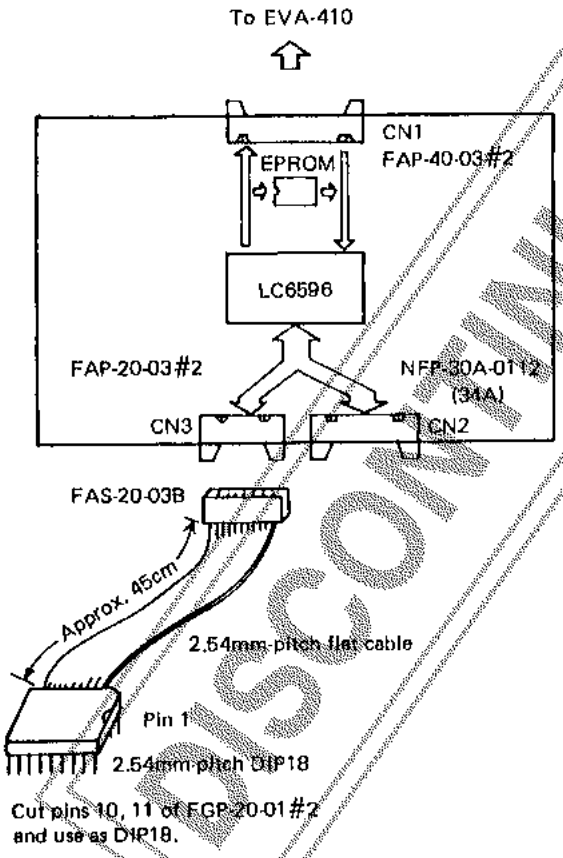


Fig. 1 Evaluation Kit Target Board (EVA-TB6523C/26C/27C/28C)

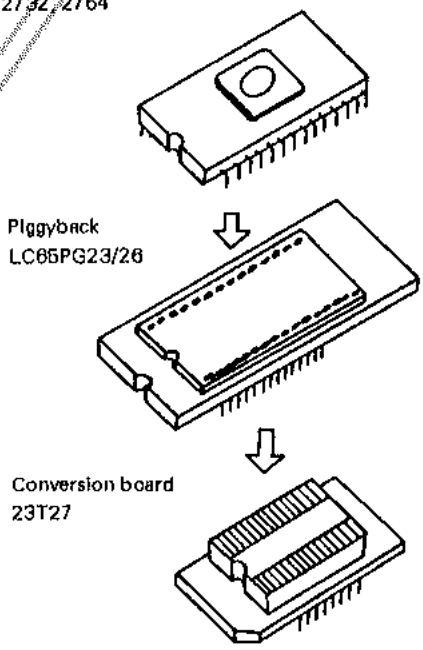
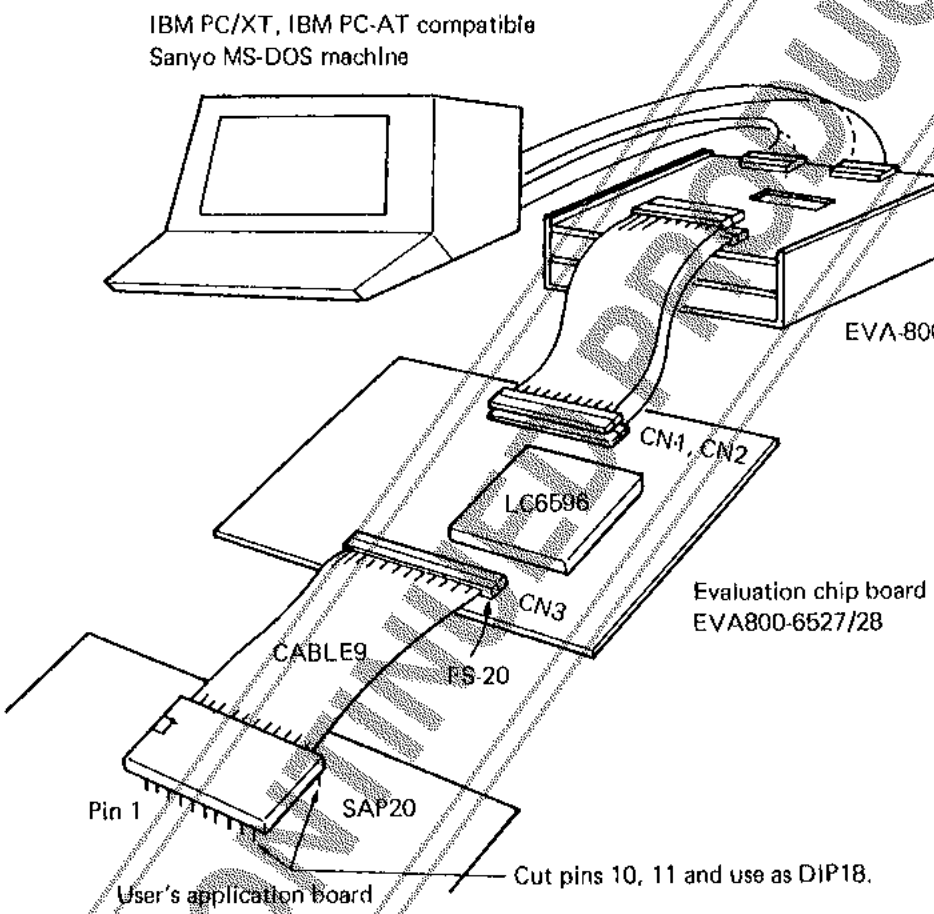


Fig. 2 For Program Evaluation

3) For program development (EVA-800 system)
   i. (IBM PC/XT, IBM PC-AT compatible Sanyo MS-DOS machine) system and cross assembler
   ii. Cross assembler ..... MS-DOS base cross assembler: (LC6527C. COM, LC6527H. COM, LC6528C. COM, LC6528H. COM)
   iii. Evaluation chip: LC6596
   iv. Emulator : EVA-800 control board and evaluation chip board (EVA800-TB6527/28)

Appearance of Development Support System



(Note 1) IBM PC/XT, IBM PC-AT: Products of IBM Corporation
MS-DOS: Trademark of Microsoft Corporation
(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B ...) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

Summary of LC6527C, LC6528C Specifications

Item			LC6527C	LC6528C
Number of basic instructions			51	51
Instruction execution time (1-word instruction) μsec			2.77 (V_{DD}=4 to6V) 6.0 (V_{DD}=3 to6V)	2.77 (V_{DD}=4 to6V) 6.0 (V_{DD}=3 to6V)
Clock frequency kHz (External drive mode)	V_{DD} 4 to6V		800 to 4330 (1/4 prescaler) 600 to 4330 (1/3 prescaler) 200 to 1444 (1/1 prescaler)	800 to 4330 (1/4 prescaler) 600 to 4330 (1/3 prescaler) 200 to 1444 (1/1 prescaler)
	V_{DD} 3 to6V		800 to 2667 (1/4 prescaler) 600 to 2000 (1/3 prescaler) 200 to 667 (1/1 prescaler)	800 to 2667 (1/4 prescaler) 600 to 2000 (1/3 prescaler) 200 to 667 (1/1 prescaler)
Memory capacity	ROM (x 8 bits)		1024	512
	RAM (x 4 bits)		64	32
Input/output ports 13 pins	A C D	Input	4 bits x 3	4 bits x 3
		Output	4 bits x 3	4 bits x 3
	H	Input	1 bit x 1	1 bit x 1
		Output	1 bit x 1	1 bit x 1
Timer			4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer
Subroutine nesting			4 levels	4 levels
Clock generator			External R, C	External R, C
			External ceramic resonator 400kHz, 800kHz, 1MHz, 4MHz	External ceramic resonator 400kHz, 800kHz, 1MHz, 4MHz
Port output characteristics	Output current		10mA typ., 20mA max., ports A,C,D,H	10mA typ., 20mA max., ports A,C,D,H
	Withstand voltage		15V (except output with pull-up resistance)	15V (except output with pull-up resistance)
Supply voltage			3 to6V	3 to6V
Package			18-pin DIP, 18-pin MFP	18-pin DIP, 18-pin MFP
Power dissipation (except port)			2.5mW (typ.) at 400kHz 12.5mW (typ.) at 4MHz	2.5mW (typ.) at 400kHz 12.5mW (typ.) at 4MHz

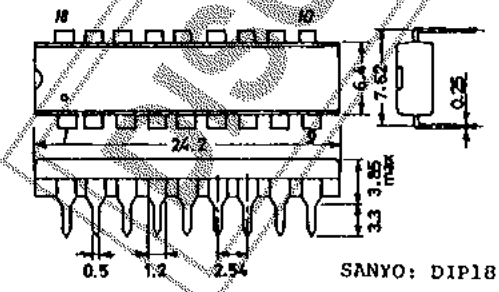
Summary of LC6527H, LC6528H Specifications

Item			LC6527H	LC6528H
Number of basic instructions			51	51
Instruction execution time (1-word instruction) μsec			0.92 (V_{DD}=4.5 to6V)	0.92 (V_{DD}=4.5 to6V)
Clock frequency kHz (External drive mode)			200 to 4330 (1/1 prescaler)	200 to 4330 (1/1 prescaler)
Memory capacity	ROM (x 8 bits)		1024	512
	RAM (x 4 bits)		64	32
Input/output ports 13 pins	A C D	Input	4 bits x 3	4 bits x 3
		Output	4 bits x 3	4 bits x 3
	H	Input	1 bit x 1	1 bit x 1
		Output	1 bit x 1	1 bit x 1
Timer			4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer
Subroutine nesting			4 levels	4 levels
Clock generator			External ceramic resonator 4MHz	External ceramic resonator 4MHz
Port output characteristics	Output current		10mA typ., 20mA max., ports A,C,D,H	10mA typ., 20mA max., ports A,C,D,H
	Withstand voltage		15V (except output with pull-up resistance)	15V (except output with pull-up resistance)
Supply voltage			4.5 to 6V	4.5 to 6V
Package			18-pin DIP, 18-pin MFP	18-pin DIP, 18-pin MFP
Power dissipation (except port)			20mW (typ.) at 4MHz	20mW (typ.) at 4MHz

Case Outline

i) DIP version

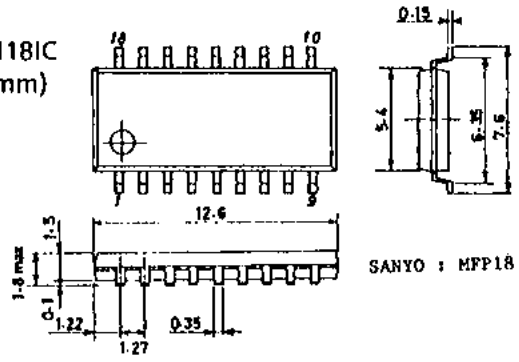
3007A-D18IC
(unit : m)



SANYO: DIP18

ii) MFP version

3095-M18IC
(unit : mm)



SANYO : MFP18

Selection Guide to Oscillator, Predivider Option

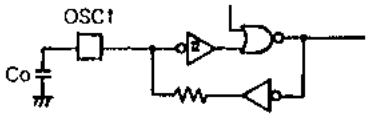
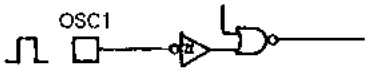
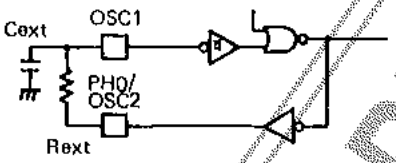
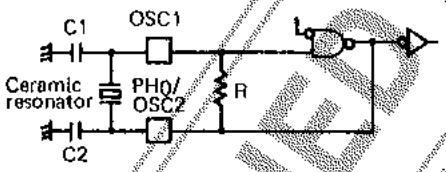
Classification for Selection			Frequency Range		Option		Remarks
C/H version	V_{DD} range	Cycle time	Clock frequency	Cycle time	OSC mode	Frequency division	
C version	3 to 6V	6 to 20μs	200 to 667kHz	6 to 20μs	1-pin external clock	1/1	
			600 to 2000kHz			1/3	
			800 to 2667kHz			1/4	
			Typ. 400kHz	Typ. 10μs	2-pin RC OSC	1/1	Possible to apply external clock
			400kHz±4%	10μs±4%	2-pin ceramic resonator OSC	1/1	Impossible to apply external clock Unusable with 1/3, 1/4 predivider
	4 to 6V	2.77 to 20μs	200 to 1444kHz	2.77 to 20 μs	1-pin external clock	1/1	
			600 to 4330kHz			1/3	
			800 to 4330kHz	3.70 to 20 μs		1/4	
			Typ. 650kHz	Typ. 6.2μs	1-pin C OSC	1/1	
			Typ. 850kHz	Typ. 4.7μs	2-pin RC OSC	1/1	Possible to apply external clock
			800kHz±4%	5μs	2-pin ceramic resonator OSC	1/1	Impossible to apply external clock
				15μs		1/3	
				20μs		1/4	
			1MHz±4%	4μs		1/1	Unusable with 1/1 predivider in 4MHz ceramic resonator OSC mode
				12μs		1/3	
				16μs		1/4	
			4MHz±4%	3μs		1/3	
				4μs		1/4	
H version	4.5 to 6.0V	0.92 to 20μs	200 to 4330kHz	0.92 to 20 μs	1-pin external clock	1/1	
			4MHz±4%	1μs	2-pin ceramic resonator OSC	1/1	Impossible to apply external clock

Pin Description

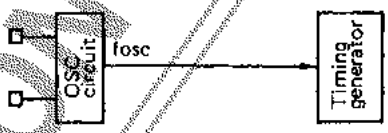
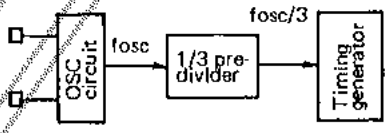
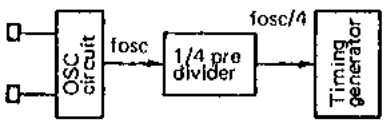
Pin Name	Pins	I/O	Function	Option	When in the Reset Mode
V_{DD}	1	—	Power supply. Normally connected to +5V.	—	—
V_{SS}	1	—	Power supply. Connected to 0V.		
OSC1	1	Input	• Pin for externally connecting C, RC, ceramic resonator for system clock generation. • For 1-pin external clock input, 1-pin C OSC, the PH_0/OSC2 pin is used as I/O port PH_0. • For 2-pin RC OSC, 2-pin ceramic resonator OSC, the PH_0/OSC2 pin is used as OSC pin OSC2.	① 1-pin external clock input ② 1-pin C OSC ③ 2-pin RC OSC ④ 2-pin ceramic resonator OSC ⑤ Predivider option 1. No predivider 2. 1/3 predivider 3. 1/4 predivider	—
PA_0 PA_1 PA_2 PA_3	4	Input/ output	• I/O port A_0 to 3. 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set/reset (SPB, RPB, instruction) • Standby is controlled by PA_3. • The PA_3 pin must be free from chattering during the HALT instruction execution cycle.	① Open drain type output ② With pull-up resistor ①, ② : Specified bit by bit	"H" output (Output Nch transistor: OFF)
PC_0 PC_1 PC_2 PC_3	4	Input/ output	• I/O port C_0 to 3. Same as for PA_0 to 3 (Note) • Option permits output at the reset mode to be "H" or "L". (Note) No standby control function is provided.	① Open drain type output ② With pull-up resistor ③ Output at the reset mode: "H" ④ Output at the reset mode: "L" • ①, ② : Specified bit by bit • ③, ④ : Specified in a group of 4 bits.	• "H" output • "L" output (Option-selectable)
PD_0 PD_1 PD_2 PD_3	4	Input/ output	• I/O port D_0 to 3. Same as for PC_0 to 3	Same as for PC_0 to 3	Same as for PC_0 to 3
PH_0/OSC2	1	Input output /output	• I/O port H_0 • Single-bit configuration • For 2-pin OSC, this pin is used as the OSC2 pin, providing no function as I/O port.	① Open drain type output ② With pull-up resistor ③ Selection of PH_0 or OSC2	"H" output (Output Nch transistor: OFF), when this pin is used as I/O port H_0.
$\overline{RES}$	1	Input	• System reset input • For power-up reset, C is connected externally. • For reset restart, "L" level is applied for 4 clock cycles or more.		
TEST	1	Input	• LSI test pin Normally connected to V_{SS}		

User Options

1) Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. 1-pin C OSC		The PH_0/PSC2 pin is used as port PH_0.
2. External clock		The PH_0/OSC2 pin is used as port PH_0.
3. 2-pin RC OSC		The PH_0/OSC2 pin is used as OSC pin OSC2, providing no function as port.
4. 2-pin ceramic resonator OSC		The PH_0/OSC2 pin is used as OSC pin OSC2, providing no function as port.

2) Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider (1/1)		• Applicable to all of 4 OSC options. • The OSC frequency, external clock do not exceed 1444kHz. (LC6527C, 6528C) • The OSC frequency, external clock do not exceed 4330kHz. (LC6527H, 6528H)
2. 1/3 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz.
3. 1/4 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz.

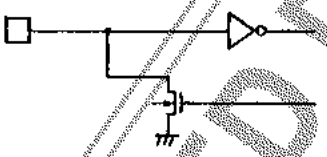
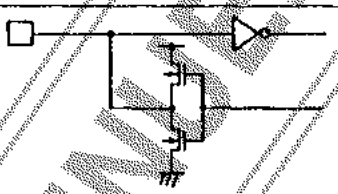
3) Option of Ports C, D Output Level at the Reset Mode

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output at the reset mode: "H"-level	All of 4 bits of ports C, D
2. Output at the reset mode: "L"-level	All of 4 bits of ports C, D

4) Option of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (Bitwise).

Option Name	Circuit	Conditions, etc.
1. Open drain output (OD)		• Unapplicable to port PH_0/OSC2 When 2-pin RC OSC or ceramic resonator OSC is selected.
2. Output with pull-up (PU)		

[LC6527C, 6528C]

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

					unit
Maximum Supply Voltage	$V_{DD}max$		V_{DD}	−0.3 to +7.0	V
Output Voltage	V_O		OSC2	−0.3 to V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC1(*1)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type	−0.3 to +15	V
	$V_{IO(2)}$		Port of PU type OSC1 for 1-pin C	−0.3 to V_{DD}+0.3	V
Peak Output Current	I_{OP}		I/O port	−2 to +20	mA
Average Output Current	I_{OA}	Per pin	I/O port	−2 to +20	mA
(Average over the period	$\Sigma I_{OA(1)}$	Total current of PA_0 to 3.	PA_0 to 3	−6 to +40	mA
of 100msec.)	$\Sigma I_{OA(2)}$	Total current of PC_0 to 3, PD_0 to 3, PH_0.	PC_0 to 3, PD_0 to 3 PH_0	−14 to +90	mA
Allowable Power Dissipation	P_{dmax}	Ta=−30 to +70°C	DIP version	400	mW
			MFP version *	275	mW
Operating Temperature	Topg			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

(*1) When oscillated internally under the oscillating conditions in Fig. 4, up to the oscillation amplitude generated is allowable.

* When mounting the MFP version on the board, do not dip it in solder.

2. Allowable Operating Conditions at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=3.0 to 6.0V unless otherwise specified

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	3.0		6.0	V
Standby Supply Voltage	V_{st}	RAM, register hold (*2)	V_{DD}	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH(1)}$	Output Nch Tr OFF	I/O port of OD type (except H_O)	0.7V_{DD}		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	I/O port of PU type (except H_O)	0.7V_{DD}		V_{DD}	V
	$V_{IH(3)}$	Output Nch Tr OFF	H_O port of OD type	0.8V_{DD}		+13.5	V
	$V_{IH(4)}$	Output Nch Tr OFF	H_O port of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH(5)}$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH(6)}$	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	Output Nch Tr OFF V_{DD}=4.0 to 6.0V	Port	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	Output Nch Tr OFF V_{DD}=3.0 to 4.0V	Port	V_{SS}		0.25V_{DD}	V
	$V_{IL(3)}$	External clock mode V_{DD}=4.0 to 6.0V	OSC1	V_{SS}		0.25V_{DD}	V
	$V_{IL(4)}$	External clock mode V_{DD}=3.0 to 4.0V	OSC1	V_{SS}		0.2V_{DD}	V
	$V_{IL(5)}$	V_{DD}=4.0 to 6.0V	TEST	V_{SS}		0.3V_{DD}	V
	$V_{IL(6)}$	V_{DD}=3.0 to 4.0V	TEST	V_{SS}		0.25V_{DD}	V
	$V_{IL(7)}$	V_{DD}=4.0 to 6.0V	$\overline{RES}$	V_{SS}		0.25V_{DD}	V
	$V_{IL(8)}$	V_{DD}=3.0 to 4.0V	$\overline{RES}$	V_{SS}		0.2V_{DD}	V

(*2) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PA_3 pin must be free from chattering during the HALT instruction execution cycle.

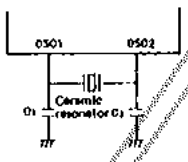
3. Electrical Characteristics at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=3.0 to 6.0V unless otherwise specified

				min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	Output Nch Tr OFF (including OFF leak current of Nch Tr) V_{IN}=+13.5V	Port of OD type			+5.0	μA
	$I_{IH(2)}$	External clock V_{IN}=V_{DD}	OSC1			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF V_{IN}=V_{SS}	Port of OD type	−1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF V_{IN}=V_{SS}	Port of PU type	−1.3	−0.35		mA
	$I_{IL(3)}$	V_{IN}=V_{SS}	$\overline{RES}$	−45	−10		μA
	$I_{IL(4)}$	External clock mode, V_{IN}=V_{SS}	OSC1	−1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50μA, V_{DD}=4.0 to 6.0V	Port of PU type	V_{DD}−1.2			V
		I_{OH}=−10μA	Port of PU type	V_{DD}−0.5			V
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA, V_{DD}=4.0 to 6.0V	Port			1.5	V
		I_{OL}=1.8mA, I_{OL} of all output pins other than any 4 output pins: 1mA or less per pin	Port			0.4	V
Hysteresis Voltage	V_{HYS}		$\overline{RES}$ OSC1 of Schmitt type (*4)		0.1V_{DD}		V
Current Dissipation (*3)							
1-Pin C Oscillation	$I_{DDOP(1)}$	Fig. 2 fosc=650kHz(typ)	V_{DD}=4 to 6V	V_{DD}	1.5	5	mA
2-Pin RC Oscillation	$I_{DDOP(2)}$	Fig. 3 fosc=850kHz(typ)	V_{DD}=4 to 6V	V_{DD}	1.5	5	mA
	$I_{DDOP(3)}$	Fig. 3 fosc=400kHz(typ)		V_{DD}	1.0	4	mA
Ceramic Resonator Oscillation	$I_{DDOP(4)}$	Fig. 4 4MHz, 1/3 predivider	V_{DD}=4 to 6V	V_{DD}	2.5	8	mA
	$I_{DDOP(5)}$	Fig. 4 4MHz, 1/4 predivider	V_{DD}=4 to 6V	V_{DD}	2.0	6	mA
	$I_{DDOP(6)}$	Fig. 4 400kHz,		V_{DD}	0.5	2	mA
	$I_{DDOP(7)}$	Fig. 4 800kHz	V_{DD}=4 to 6V	V_{DD}	1.5	4	mA
External Clock	$I_{DDOP(8)}$	200kHz to 667kHz, 1/1 predivider 600kHz to 2000kHz, 1/3 predivider 800kHz to 2667kHz, 1/4 predivider		V_{DD}	1.5	5	mA
	$I_{DDOP(9)}$	200kHz to 1444kHz, 1/1 predivider 600kHz to 4330kHz, 1/3 predivider 800kHz to 4330kHz, 1/4 predivider	V_{DD}=4 to 6V	V_{DD}	2.5	8	mA
Standby Mode	I_{DDst}		V_{DD}=6V	V_{DD}	0.05	10	μA
			V_{DD}=3V	V_{DD}	0.025	5	μA
I/O Port Pull-up Resistance	R_{PP}		V_{DD}=5V, Port of PU type		14		kohm
External Reset Characteristics							
Reset Time	t_{RST}				See Fig. 6.		
Pin Capacitance	C_P	f=1MHz, other than pins to be tested, V_{IN}=V_{SS}			10		pF

(*3) The current dissipation is specified under the following conditions.
- Output Nch transistor OFF, port=V_{DD}.

(*4) The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

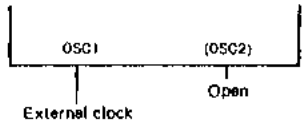
4. Allowable Conditions of Clock Generator at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=3.0 to 6.0V unless otherwise specified

				min	typ	max	unit
Clock Input Frequency	f_{op}	1/1 predivider option (N=1)	OSC1	200		1400	kHz
(Cycle Time T_{CYC})	(T_{CYC})	V_{DD}=4.0 to 6.0V		(20)		(2.77)	(μs)
$T_{CYC}=(4/f_{op})\cdot N$		1/1 predivider option (N=1)	OSC1	200		667	kHz
N: Number of divisions		V_{DD}=3.0 to 6.0V		(20)		(6.0)	(μs)
		1/3 predivider option (N=3)	OSC1	600		4330	kHz
		V_{DD}=4.0 to 6.0V		(20)		(2.77)	(μs)
		1/3 predivider option (N=3)	OSC1	600		2000	kHz
		V_{DD}=3.0 to 6.0V		(20)		(6.0)	(μs)
		1/4 predivider option (N=4)	OSC1	768		4330	kHz
		V_{DD}=4.0 to 6.0V		(20.8)		(3.81)	(μs)
		1/4 predivider option (N=4)	OSC1	768		2667	kHz
		V_{DD}=3.0 to 6.0V		(20.8)		(6.0)	(μs)
"H"/"L"-Level Input Pulse Width of External Clock Input	t_{extH}	Fig. 1 V_{DD}=4.0 to 6.0V	OSC1	69			ns
	t_{extL}	Fig. 1 V_{DD}=3.0 to 6.0V	OSC1	180			ns
Rise/Fall Time of External Clock Input	t_{extR}	Fig. 1 V_{DD}=4.0 to 6.0V	OSC1			50	ns
	t_{extF}	Fig. 1 V_{DD}=3.0 to 6.0V	OSC1			100	ns
OSC Guaranteed Constant (1-Pin C OSC)	C_o	Fig. 2 V_{DD}=4.0 to 6.0V	OSC1	150±5%			pF
OSC Guaranteed Constant (2-Pin RC OSC)	C_{ext}	Fig. 3 V_{DD}=3.0 to 6.0V	OSC1, OSC2	270±5%			pF
	Rext	Fig. 3 V_{DD}=3.0 to 6.0V	OSC1, OSC2	12±1%			kohm
	C_{ext}	Fig. 3 V_{DD}=4.0 to 6.0V	OSC1, OSC2	220±5%			pF
	R_{ext}	Fig. 3 V_{DD}=4.0 to 6.0V	OSC1, OSC2	5.6±1%			kohm
OSC Guaranteed Constant (Ceramic Resonator OSC)		V_{DD}=3.0 to 6.0V 400kHz ceramic resonator OSC	OSC1, OSC2	For ceramic resonator, C1, C2, refer to Table 1.			
		V_{DD}=4.0 to 6.0V 800kHz, 1000kHz 4MHz ceramic resonator OSC	OSC1, OSC2				

5. Electrical Characteristics of Clock Generator at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=3.0 to 6.0V unless otherwise specified

				min	typ	max	unit
Ceramic Resonator OSC							
OSC Frequency	f_{CFOSC} (*5)	Fig. 4 fo=400kHz	OSC1, OSC2	384	400	416	kHz
		Fig. 4 fo=800kHz V_{DD}=4 to 6V	OSC1, OSC2	768	800	832	kHz
		Fig. 4 fo=1MHz V_{DD}=4 to 6V	OSC1, OSC2	960	1000	1040	kHz
		Fig. 4 fo=4MHz, 1/3 predivider, 1/4 predivider V_{DD}=4 to 6V	OSC1, OSC2	3840	4000	4160	kHz
OSC Stabilizing Time	t_{CFS}	Fig. 5 fo=400kHz				10	ms
		Fig. 5 fo=800kHz, 1MHz, 4MHz, 1/3 predivider, 1/4 predivider V_{DD}=4 to 6V				10	ms
1-Pin C OSC OSC Frequency	f_{COSC}	Fig. 2 Co=150pF±5% V_{DD}=4 to 6V	OSC1	320	650	1360	kHz
2-Pin RC OSC OSC Frequency	f_{MOSC}	Fig. 3 Cext=220pF±5% Fig. 3 Rext=5.6kohm±1% V_{DD}=4 to 6V	OSC1, OSC2	600	850	1235	kHz
		Fig. 3 Cext=270pF±5% Fig. 3 Rext=12kohm±1%	OSC1, OSC2	260	400	645	kHz

(*5) f_{CFOSC}: Oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.



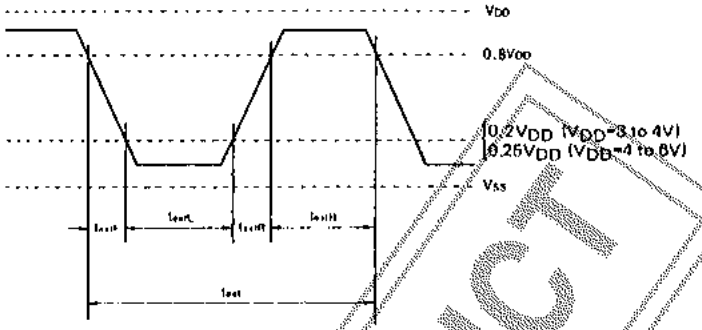


Fig. 1 External Clock Input Waveform

* The external clock can be used only when the 2-pin RC option or 1-pin external clock option is selected and cannot be used when the ceramic resonator OSC option is selected.

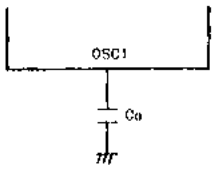


Fig. 2 1-Pin C Oscillation Circuit

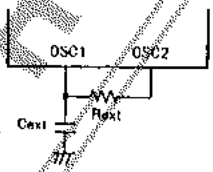


Fig. 3 2-Pin RC Oscillation Circuit

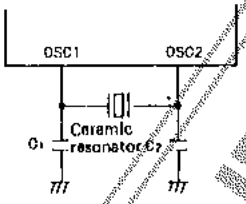


Fig. 4 Ceramic Resonator Oscillation Circuit

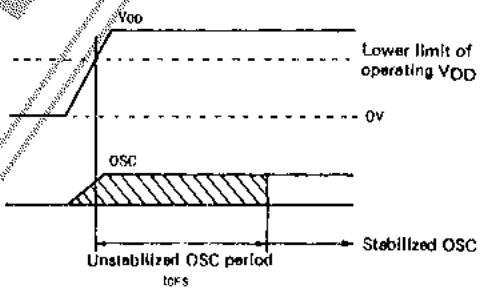


Fig. 5 Oscillation Stabilizing Period

4MHz	CSA4.00MG (Murata)	C1	30pF±10%
		C2	30pF±10%
	KBR4.0M (Kyocera)	C1	33pF±10%
		C2	33pF±10%
1MHz	CSB1000D (Murata)	C1	100pF±10%
		C2	100pF±10%
	KBR1000H (Kyocera)	C1	100pF±10%
		C2	100pF±10%
800kHz	CSB800D (Murata)	C1	100pF±10%
		C2	100pF±10%
	KBR800H (Kyocera)	C1	100pF±10%
		C2	100pF±10%
400kHz	CSB400P (Murata)	C1	330pF±10%
		C2	330pF±10%
	KBR400B (Kyocera) KBR400H	C1	150pF±10%
		C2	150pF±10%

Table 1 Constants Guaranteed for Ceramic Resonator OSC

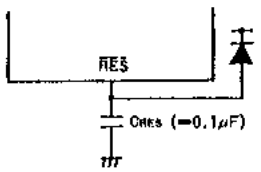


Fig. 6 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF.
If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

RC Oscillation Characteristic of the LC6527, 6528 (when the 2-pin RC OSC option is selected)
Fig. 7 shows the RC oscillation characteristic of the LC6527, 6528. For the variation range of RC OSC frequency of the LC6527, 6528, the following are guaranteed at the external constants only shown below.

i) V_{DD}=3.0V to 6.0V, Ta=−30°C to +70°C
External constants Cext=270pF
Rext=12kohms
260kHz≦fmosc≦645kHz

ii) V_{DD}=4.0V to 6.0V, Ta=−30°C to +70°C
Cext=220pF
Rext=5.6kohms
600kHz≦fmosc≦1235kHz

If any other constants than specified above are used, the range of Rext=3kohms to 20kohms, Cext=150pF to 390pF must be observed. (See Fig. 7.)

The oscillation frequency at V_{DD}=5.0V, Ta=+25°C must be in the range of 400kHz to 850kHz.
The oscillation frequency at V_{DD}=4.0V to 6.0V, Ta=−30°C to +70°C and V_{DD}=3.0V to 6.0V, Ta=−30°C to +70°C must be within the operation clock frequency range (Table of OSC, Predivider Option).

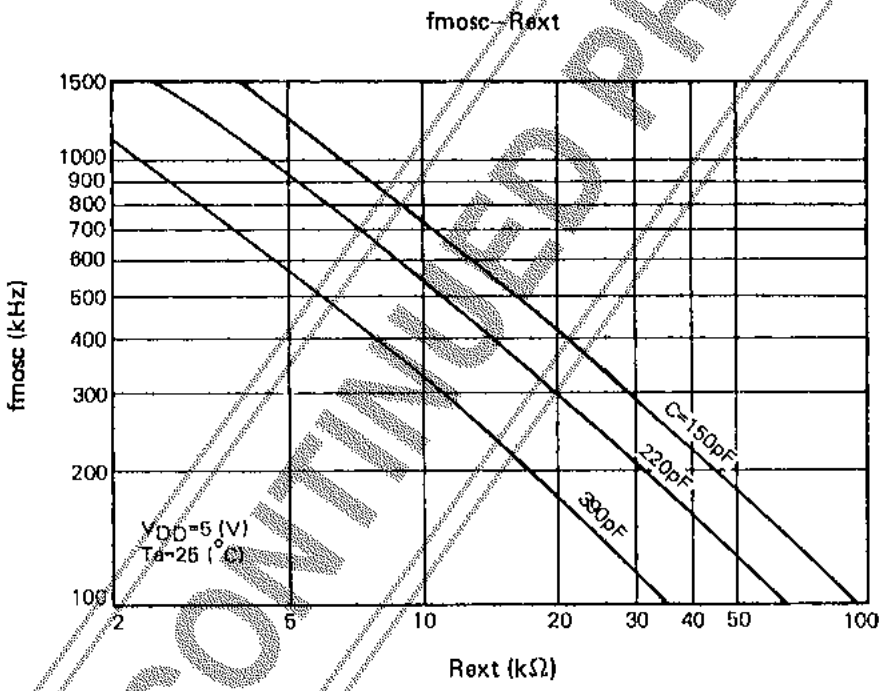


Fig. 7 2-Pin RC Oscillation Frequency Data (Typ.)

[LC6527H, 6528H]

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

					unit
Maximum Supply Voltage	$V_{DD}max$		V_{DD}	−0.3 to +7.0	V
Output Voltage	V_O		OSC2	−0.3 to V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC1 (*1)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type	−0.3 to +15	V
	$V_{IO(2)}$		Port of PU type	−0.3 to V_{DD}+0.3	V
			OSC1 for 1-pin C OSC		
Peak Output Current	I_{OP}		I/O port	−2 to +20	mA
Average Output Current	I_{OA}	Per pin	I/O port	−2 to +20	mA
(Average over the period	$\Sigma I_{OA(1)}$	Total current of PA_0 to 3,	PA_0 to 3	−6 to +40	mA
of 100msec.)	$\Sigma I_{OA(2)}$	Total current of PC_0 to 3, PD_0 to 3, PH_0	PC_0 to 3, PD_0 to 3, PH_0	−14 to +90	mA
Allowable Power Dissipation	Pdmax	Ta=−30 to +70°C	DIP version	400	mW
			MFP version *	275	mW
Operating Temperature	Topg			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

(*1) When oscillated internally under the oscilating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.

* When mounting the MFP version on the board, do not dip it in solder.

2. Allowable Operating Conditions at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 6.0V

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.5		6.0	V
Standby Supply Voltage	V_{st}	RAM, register hold (*2)	V_{DD}	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH(1)}$	Output Nch Tr OFF	Port of OD type (except H_0)	0.7V_{DD}		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of PU type (except H_0)	0.7V_{DD}		V_{DD}	V
	$V_{IH(3)}$	Output Nch Tr OFF	H_0 of OD type	0.8V_{DD}		+13.5	V
	$V_{IH(4)}$	Output Nch Tr OFF	H_0 of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH(5)}$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH(6)}$	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	Output Nch Tr OFF	Port	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	External clock mode	OSC1	V_{SS}		0.25V_{DD}	V
	$V_{IL(3)}$		TEST	V_{SS}		0.3V_{DD}	V
	$V_{IL(4)}$		$\overline{RES}$	V_{SS}		0.25V_{DD}	V
Operating Frequency	fop			200		4330	kHz
(Cycle Time)	(t_{CYC})			(20)		(0.92)	(μs)
External Clock Conditions							
Frequency	f_{ext}	Fig. 1	OSC1	200		4330	kHz
Pulse Width	t_{extH}	Fig. 1	OSC1	69			ns
	t_{extL}	Fig. 1					
Rise/Fall Time	t_{extR}	Fig. 1	OSC1			50	ns
	t_{extF}	Fig. 1					
Oscillation Guaranteed Constants							
Ceramic Resonator Oscillation		Fig. 2		For ceramic resonator, C1, C2, see Table 1.			

(*2) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PA_3 pin must be free from chattering during the HALT instruction execution cycle.

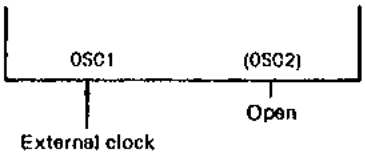
3. Electrical Characteristics at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 6.0V unless other wise specified

				min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	Output Nch Tr OFF (including OFF leak current of Nch Tr) V_{IN}=+13.5V	Port of OD type			+5.0	μA
	$I_{IH(2)}$	External clock mode, $V_{IN}=V_{DD}$	OSC1			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of OD type	−1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of PU type	−1.3	−0.35		mA
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	−45	−10		μA
	$I_{IL(4)}$	External clock mode, $V_{IN}=V_{SS}$	OSC1	−1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50μA	Port of PU type	V_{DD}−1.2			V
		I_{OH}=−10μA	Port of PU type	V_{DD}−0.5			V
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA	Port			1.5	V
		I_{OL}=1.8mA, I_{OL} of all output pins other than any 4 output pins: 1mA or less per pin	Port			0.4	V
Hysteresis Voltage	V_{HYS}		$\overline{RES}$		0.1V_{DD}		V
			OSC1 of Schmitt type (*5)				
Current Dissipation (*3)							
Ceramic Resonator Oscillation	$I_{DDOP(1)}$	Fig. 2 4MHz	V_{DD}		4.0	10	mA
External Clock	$I_{DDOP(2)}$	200kHz to 4330kHz	V_{DD}		4.0	10	mA
Standby Mode	I_{DDSt}		V_{DD}=6V V_{DD}		0.05	10	μA
			V_{DD}=3V V_{DD}		0.025	5	μA
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC}	Fig. 2, fo=4MHz (*4)	OSC1, OSC2	3840	4000	4160	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 3, fo=4MHz				10	ms
I/O Port Pull-up Resistance	R_{PP}		V_{DD}=5V, Port of PU type		14		kohm
External Reset Characteristics							
Reset Time	t_{RST}				See Fig. 4.		
Pin Capacitance	C_P	f=1MHz, other than pins to be tested, $V_{IN}=V_{SS}$			10		pF

(*3) The current dissipation is specified under the following conditions.
- Output Nch transistor OFF, port=V_{DD}.

(*4) f_{CFOSC}: Oscillatable frequency

(*5) The OSC1 becomes the Schmitt type when the OSC option is the external clock OSC.



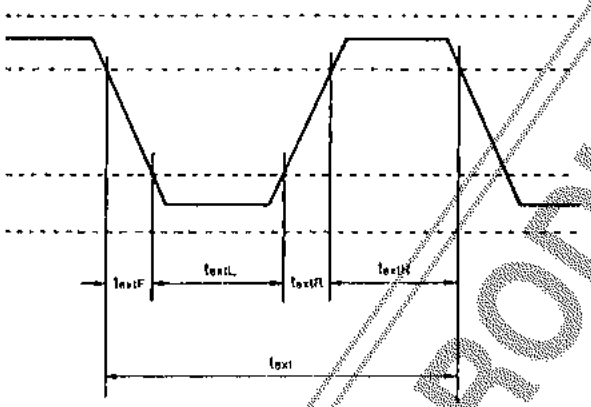


Fig. 1 External Clock Input Waveform

* The external clock can be used only when the 1-pin external clock option is selected and cannot be used when the ceramic resonator OSC option is selected.

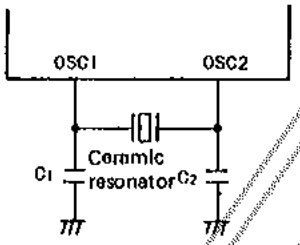


Fig. 2 Ceramic Resonator Oscillation Circuit

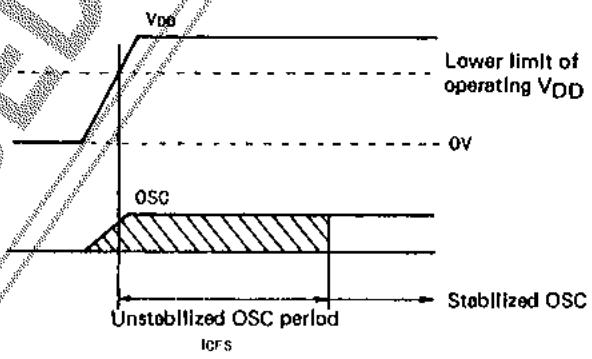


Fig. 3 Oscillation Stabilizing Period

4MHz	CSA4.00MG (Murata)	C1	30pF±10%
		C2	30pF±10%
	KBR4.0M (Kyocera)	C1	33pF±10%
		C2	33pF±10%

Table 1 Constants Guaranteed for Ceramic Resonator OSC

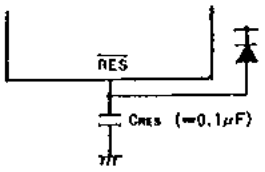


Fig. 4 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF.
If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

Notes for Program Evaluation

- When evaluating the LC6527/28 with the evaluation chip (LC6596, LC65PG23/26), the following must be observed.

Classification	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for option	2-pin OSC	PH_0 and OSC2 share one pin (PH_0/OSC2). Either of them is selected exclusively by user option. When 2-pin OSC is selected, PH_0/OSC2 pin provides OSC2 and performs no function as PH_0 port. Data input to PH_0/OSC2 by mistake is always read as "0".	Evaluation chip has PH_0 and OSC2 separately. Pin required for option is selected as required. Even when OSC2 pin is selected by option, PH_0 circuit is present and functions as complete port PH_0.	Since input/output at PH_0 on evaluation chip results in difference between evaluation chip operation and mass-production chip operation, input/output at PH_0 is prohibited.
	1-pin OSC	When 1-pin C OSC is selected, OSC circuit is formed by connecting catalog guranteed C to OSC1 pin.	Since no OSC circuit for 1-pin C OSC is contained, 1-pin C OSC is not available.	2-pin RC provides OSC and frequency is adjusted as desired. OSC characteristic differs, but there is no restriction on program (ES, CS must be used to evaluate OSC characteristic in detail).
	OSC predivider	3 selections (1/1, 1/3, 1/4) by option.	3 selections (1/1, 1/3, 1/4) available by 2 pins of DIV pin, 3OR4 pin.	DIV pin, 3OR4 pin must be set according to option specified for mass-production chip.
	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and port D can be brought to "H" and "L" by CHL pin and DHL pin respectively.	CHL pin and DHL pin must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected bitwise.	Only OD without PU.	[LC6596-applied evaluation] External resistor (15kohms) on evaluation board must be connected to necessary port. [Piggyback-applied evaluation] Resistor must be connected to necessary port on application board.
	PU resistor configuration	PU resistor brought to Hi-Z (Pch Tr to turn OFF) at "L" output mode.	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode.	For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.
Notes for OSC	OSC constants -1	[2-pin RC OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin RC OSC] Different from mass-production chip in circuit design and characteristic.	[2-pin RC OSC] Frequency must be adjusted to OSC frequency of mass-production chip by adjusting variable resistor.
		[2-pin ceramic resonator OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin ceramic resonator OSC] Different from mass-production chip in circuit design and characteristic. Wiring capacitance may provide unstable OSC.	[2-pin ceramic resonator OSC] External constants must be fine-adjusted according to service conditions.
	OSC constants -2 (Note)	[2-pin ceramic resonator OSC] Feedback resistor is contained.	[2-pin ceramic resonator OSC] No feedback resistor is contained.	[2-pin ceramic resonator OSC] For evaluation chip, feedback resistor of 1Mohm must be connected externally.

Continued on next page.

Continued from preceding page.

Classification	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for electrical characteristics	OSC frequency	OSC frequency characteristic as indicated in catalog.	Different from mass-production chip in circuit design, and characteristic.	ES, CS must be used to evaluate characteristic in detail.
	Operating current, standby current	Current characteristic as indicated in catalog.	Different from mass-production chip in circuit design, characteristic.	
Other notes	Type No. setting	LC6527/28 differ in ROM, RAM.	ROM, RAM to be used according to Type No. are set by INSTC, MEMC.	INSTC, MEMC are set according to Type No. of mass-production chip.
	Evaluation chip pin setting		Input pin RSTC, which is not provided in mass-production chip, is provided.	SW4 on evaluation board must remain turned OFF.

Note) When the evaluation chip is used in the 2-pin ceramic resonator OSC mode, no feedback resistor is contained unlike the mass-production chip. Connect a feedback resistor of 1Mohm externally as shown below.
Since constants R, C are also differ from those for the mass-production chip, refer to Table 1 and adjust the capacitor value according to the stray capacitance of the circuit.

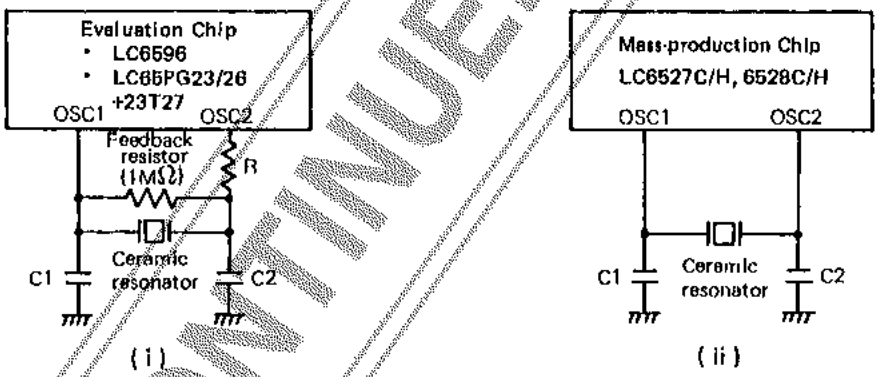


Fig. 1 2-Pin Ceramic Resonator OSC Circuit for Evaluation Chip and Mass-production Chip

Ceramic resonator		Mass-production chip C1=C2	Evaluation chip (*)			
			Including capacitance of standard cable(FAS-20-03B)		Including no capacitance of standard cable(FAS-20-03B)	
			C1=C2	R	C1=C2	R
4MHz	CSA4.00MG (Murata)	30pF	8pF	0Ω	33pF	0Ω
	KBR4.0M (Kyocera)	33pF	8pF	0Ω	33pF	0Ω
1MHz	CSB1000K (Murata)	(Using CSB1000D) 100pF	82pF	2.2kΩ	100pF	2.2kΩ
	KBR1000H (Kyocera)	100pF	82pF	2.2kΩ	100pF	2.2kΩ
800kHz	CSB800K (Murata)	(Using CSB800D) 100pF	120pF	2.2kΩ	150pF	2.2kΩ
	KBR800H (Kyocera)	100pF	120pF	2.2kΩ	150pF	2.2kΩ
400kHz	CSB400P (Murata)	330pF	220pF	3.3kΩ	270pF	3.3kΩ
	KBR400B (Kyocera) KBR400H	150pF	330pF	1.0kΩ	330pF	1.0kΩ

Table 1 Reference Values of Constants R, C

(*) Standard cable (FAS-20-03B) is a cable attached to target board EVA-TB6523C/26C/27C/28C.
Table 1 shows two cases where the capacitance of the cable is included and no capacitance of the cable is included.

- Example where the capacitance of the cable is included
  The capacitance of the cable is included when the resonator is connected to the user's application board through the cable from the EVA-TB6523C/26C/27C/28C.
- Example where no capacitance of the cable is included
  No capacitance of the cable is included when the resonator is placed near the evaluation chip (on the EVA-TB6523C/26C/27C/28C).

When using any other cable than the attached cable, adjust the capacitor value according to the stray capacitance.

LC6527, 6528 INSTRUCTION SET (BY FUNCTION)

Symbol	Description				
AC	: Accumulator	P(DP_L)	: Input/output port addressed by DP_L	( ), [ ]	: Contents
ACt	: Accumulator bit t	PC	: Program counter	←	: Transfer and direction
CF	: Carry flag	STACK	: Stack register	+	: Addition
DP	: Data pointer	TM	: Timer	−	: Subtraction
E	: E register	TMF	: Timer (interval) interrupt request flag	∨	: Exclusive OR
M	: Memory	ZF	: Zero flag		
M(DP)	: Memory addressed by DP				

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	*1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇄ (E)	The AC contents and the E contents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← (M(DP)) + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← (M(DP)) − 1	The M(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 1	A single bit of the M(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 0	A single bit of the M(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{(M(DP))}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset.	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset.	ZF CF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	*1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	The M(DP) contents are loaded in the AC.	ZF	
Data pointer manipulation instructions	LDZ data	Load DP_H with zero and DP_L with immediate data respectively	1 0 0 0	$I_3I_2I_1I_0$	1	1	DP_H ← 0 DP_L ← $I_3I_2I_1I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3I_2I_1I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	0 0 I_1I_0	1	1	DP_H ← I_1I_0	The DP_H is loaded with the immediate data I_1I_0.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	DP_L ← (DP_L) + 1	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	DP_L ← (DP_L) − 1	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	DP_L ← (AC)	The AC contents are transferred to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	AC ← (DP_L)	The DP_L contents are transferred to the AC.	ZF	
Jump/subroutine instructions	JMP addr	Jump	0 1 1 0 $P_7P_6P_5P_4$	1 0 P_9P_8 $P_3P_2P_1P_0$	2	2	PC ← $P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$	A jump to the address specified with immediate data $P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$ occurs		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3P_2P_1P_0$	1	1	STACK ← (PC) + 1 $PC_{9\sim6}$, $PC_{1\sim0}$ ← 0 $PC_{5\sim2}$ ← $P_3P_2P_1P_0$	A subroutine in page 0 is called.		
	CAL addr	Call subroutine	1 0 1 0 $P_7P_6P_5P_4$	1 0 P_9P_8 $P_3P_2P_1P_0$	2	2	STACK ← (PC) + 2 $PC_{9\sim0}$ ← $P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$	A subroutine is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.		

Comparison result	CF	ZF
(M(DP)) > (AC)	0	0
(M(DP)) = (AC)	1	1
(M(DP)) < (AC)	1	0

Comparison result	CF	ZF
$I_3I_2I_1I_0$ > (AC)	0	0
$I_3I_2I_1I_0$ = (AC)	1	1
$I_3I_2I_1I_0$ < (AC)	1	0

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
	BAt addr	Branch on AC bit	0 1 1 1 $P_7P_6P_5P_4$	0 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ACt = 1	If a single bit of the AC specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7P_6P_5P_4$	0 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ACt = 0	If a single bit of the AC specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7P_6P_5P_4$	0 1 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (M(DP).t_1t_0) = 1	If a single bit of the M(DP) specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7P_6P_5P_4$	0 1 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (M(DP.t_1t_0) = 0	If a single bit of the M(DP) specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7P_6P_5P_4$	1 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (P(DP$_L$.t_1t_0) = 1	If a single bit of port P(DP$_L$) specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7P_6P_5P_4$	1 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (P(DP$_L$.t_1t_0) = 0	If a single bit of port P(DP$_L$) specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BC addr	Branch on CF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← P(DP$_L$)	Port P(DP$_L$) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP$_L$) ← (AC)	The AC contents are outputted to port P(DP$_L$).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1B_0	1	2	P(DP$_L$.B_1B_0) ← 1	A single bit in port P(DP$_L$) specified with the immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1B_0	1	2	P(DP$_L$.B_1B_0) ← 0	A single bit in port P(DP$_L$) specified with the immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E).(AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		Only when all pins of port PA are set at L, stop.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used continuously in such a manner as CLA, CLA, ———, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

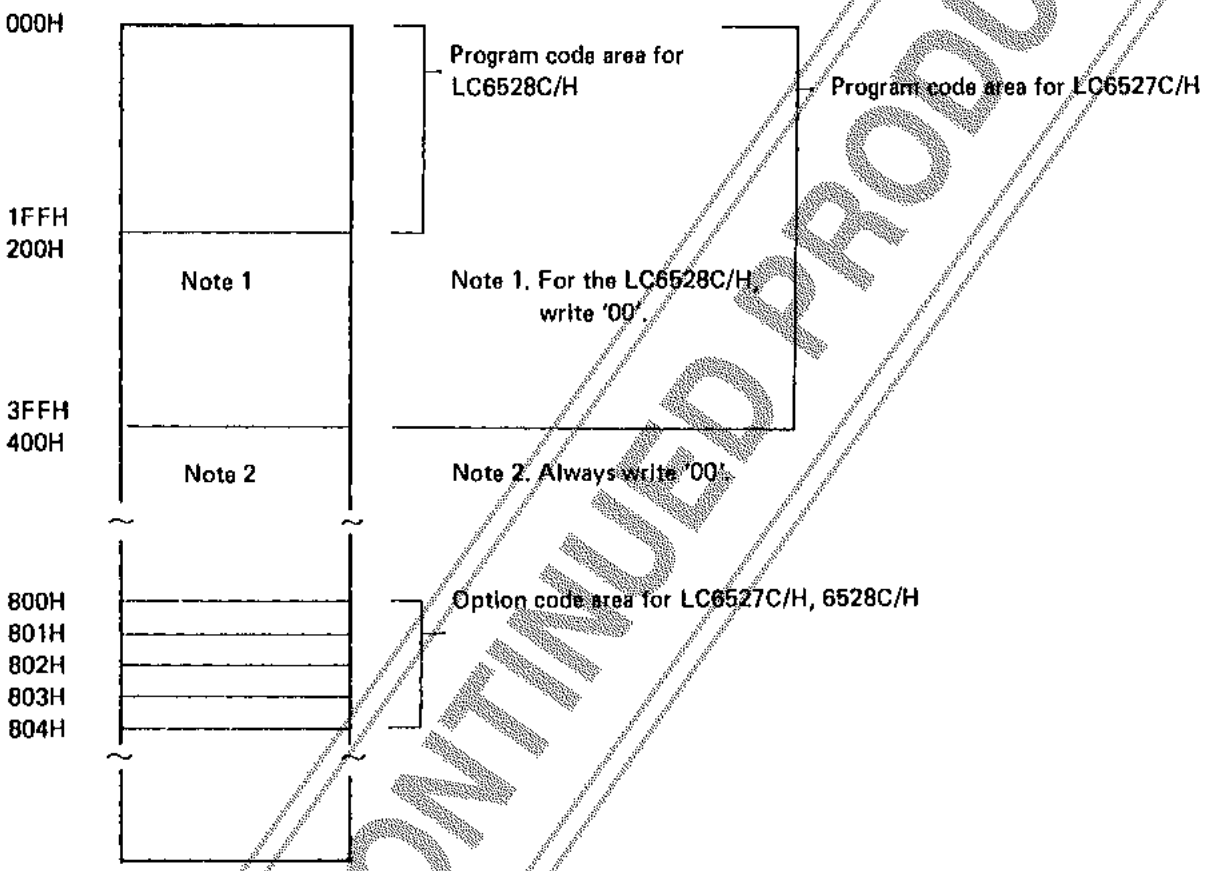
(The following instructions, which are included in the instruction set of the LC6523, 6526, are excluded:
AND, BFn, BI, BNFn, BNI, CLI, JPEA, OR RAL, RCTL, RFB, RTI, RTBL, SCTL, SFB, X, XAH, XA0, XA1, XA2, XA3, XD, XH0, XH1, XI, XL0, XL1, XM)

LC6527C/H, 6528C/H Option Code Specifying Method

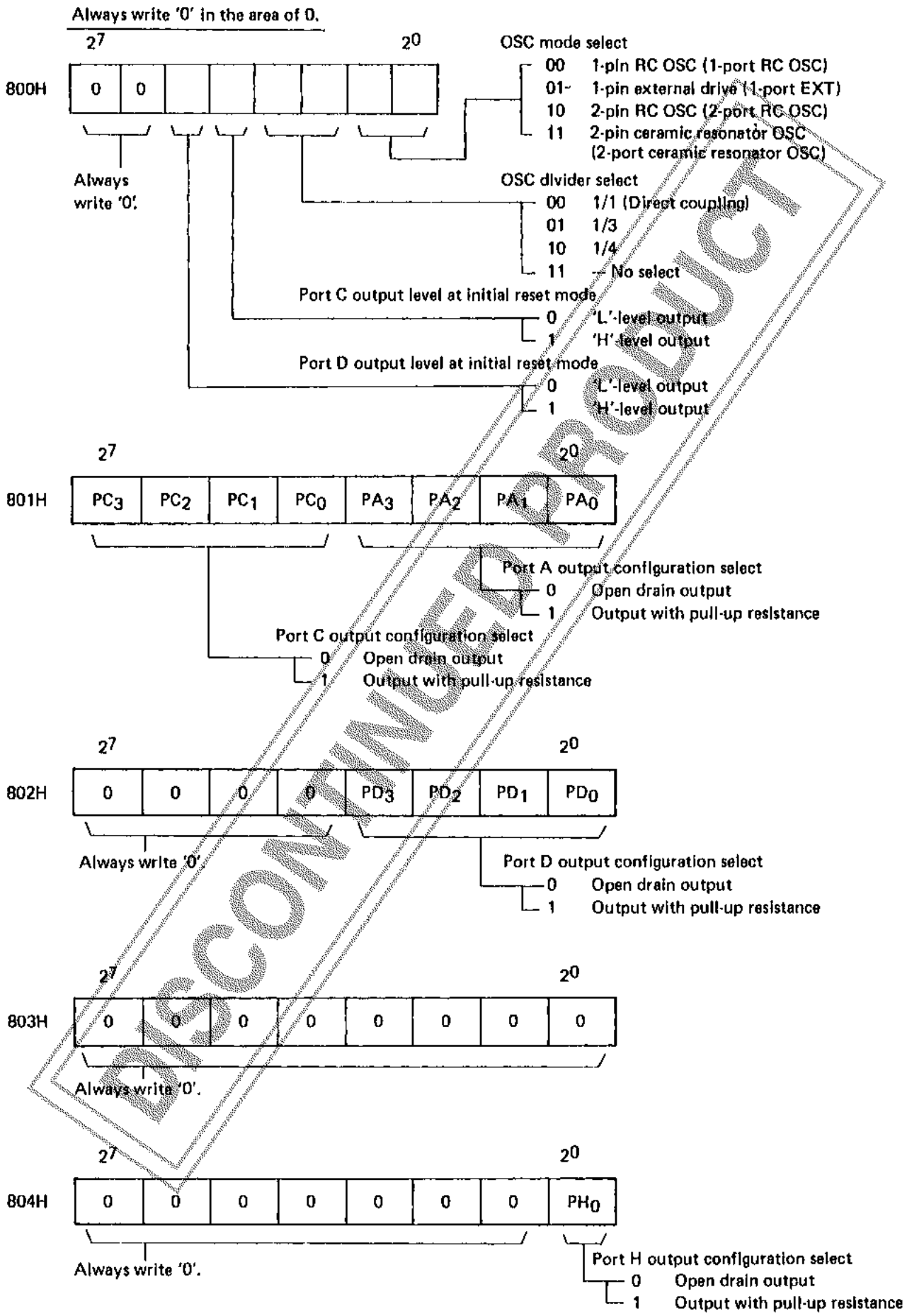
General.Description

It is requested that you should submit to us various mask options of the LC6527C/H, LC6528C/H together with the program code which are stored in an EPROM.
By using our cross assembler for the LC6527, 6528, the option code can be specified interactively and stored in the EPROM.
If our cross assembler is not used, specify the option code as shown below. (This is the same as the method where the cross assembler is created automatically.)

The Type No. of the EPROM to be submitted is 2732 or 2764.

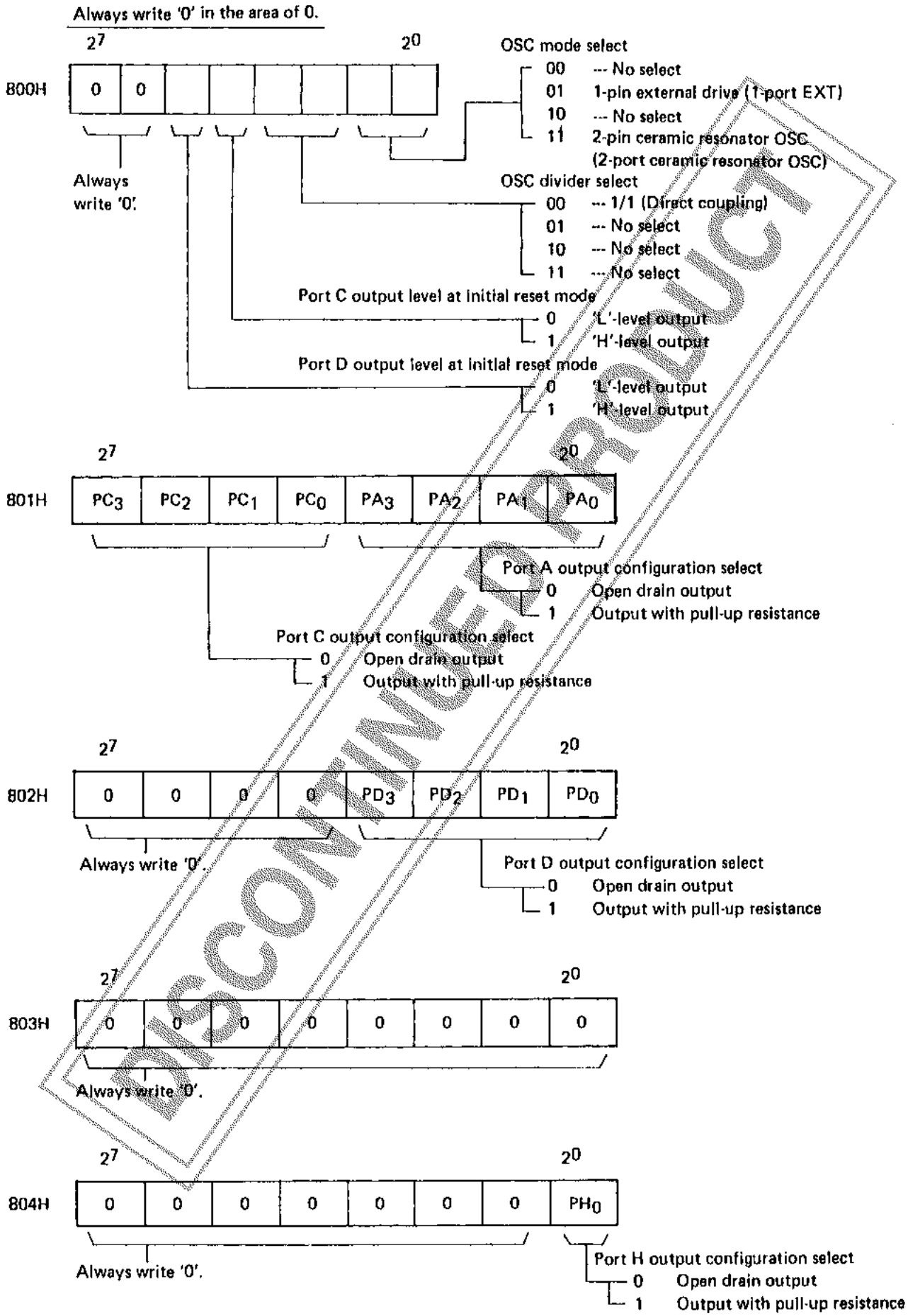


C Version (LC6527C, LC6528C) Option Code Specifying Method



Note: When the 2-pin OSC mode is selected, always write '0'.

H Version (LC6527H, LC6528H) Option Code Specifying Method



Note: When the 2-pin OSC mode is selected, always write '0'.

Notes for Standby Function Application

The LC6527C/H, 6528C/H provide the standby function called HALT mode to minimize the current dissipation when the program is in the wait state.

The standby function is controlled by the HALT instruction, PA pin, $\overline{RES}$ pin.

A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed. This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below.

When using the standby function, the application circuit shown below must be used and the notes must be also fully observed.

If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of application equipment.

1. HALT mode release conditions

   The HALT mode setting, release conditions are shown in Table 1.

Table 1 HALT mode setting, release conditions

HALT mode setting conditions	HALT mode release conditions
HALT instruction Provided that PA_3 is at high level.	① Reset (Low level is applied to $\overline{RES}$.) ② Low level is applied to PA_3.

Note) HALT mode release condition ② is available only when the RC mode is used for system clock generation; and unavailable when the ceramic resonator mode is used because the OSC circuit may not operate normally.

2. Proper cares in using standby function

   When using the standby function, an application circuit and program must be designed with the following in mind.

   (1) The supply voltage at the standby state must not be less than specified.
   (2) Input timing and conditions of each control signal ($\overline{RES}$, PA_3) must be observed at the standby initiate/release state.
   (3) Release operation must not be overlapped at the time of execution of the HALT instruction.

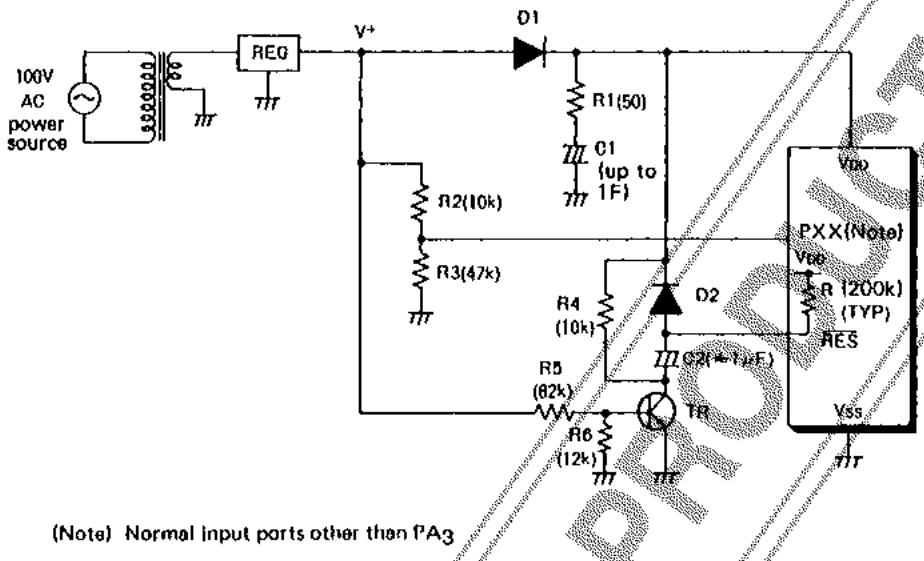
   A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

   Sample application where the standby function is used for power failure backup.

   Power failure backup is an application where power failure of the main power source is detected and the HALT instruction is executed to cause the standby state to be entered. The power dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers for a certain period of time. After power is restored, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC). Shown below are sample applications where the program selects or not between power-ON reset and reset after power is restored, notes, measures for instantaneous break of AC power.

2-1. Sample application 1 where the standby function is used for power failure backup
Shown below is a sample application where the program does not select between power-ON reset and reset after power is restored.

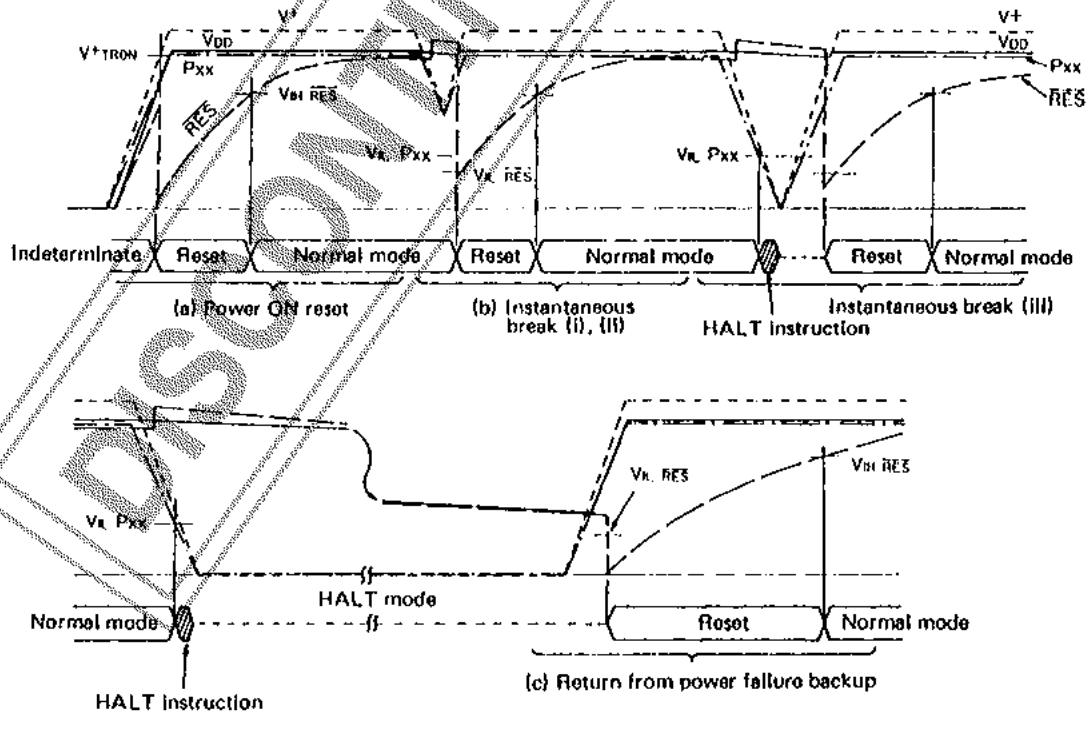
2-1-1. Sample application circuit — (1)
Fig. 2-1 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA3

Fig. 2-1. Sample application — (1) where the standby function is used for power failure backup

2-1-2. Operating waveform in sample application circuit — (1)
The operating waveform in the sample application circuit in Fig. 2-1 is shown in Fig. 2-2. The mode is roughly divided as follows:
(a) Power-ON reset
(b) Instantaneous break of main power source
(c) Return from power failure backup



V^{+}_{TRON}: V^{+} value when TR is turned ON/OFF

Fig. 2-2 Operating waveform in sample application circuit — (1)

2-1-3. Operation of sample application circuit – (1)

(a) At the time of power-ON reset

After power rises, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC).

– Note –

This sample application circuit provides an indeterminate region where no reset occurs before the operating V_{DD} range is entered.

(b) At the time of instantaneous break

(i) When the P_{XX} input voltage does not meet V_{IL} (the P_{XX} input level does not get lower than input threshold level V_{IL}) and the $\overline{RES}$ input voltage only meets V_{IL}:
A reset occurs in the normal mode, providing the same operation as power-ON reset.

(ii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage meet V_{IL}:
When two pollings do not regard the P_{XX} input voltage as "L" level, the HALT mode is not entered and reset occurs.
When two pollings regard the P_{XX} input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode.

(c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

2-1-4. Notes for design of sample application circuit – (1)

- V^+ rise time and C2
  Make the time constant (C2, R) of the reset circuit 10 times as long as the V^+ rise time. (R: ON-chip resistor, 200kohms typ.)
  Make the V^+ rise time shorter (up to 20ms).
- R1 and C1
  Make the R1 value as small as possible. Make the C1 value as large as possible according to the backup time calculated. (Fix the R1 value so that the C1 charging current does not exceed the power source capacity.)
- R2 and R3
  Make the "H"-level input voltage applied to the P_{XX} pin equal to V_{DD}.
- R4
  Fix the time constant of C2 and C4 so that C2 can discharge during the period of time from when V^+ gets lower than $V^+_{TRON(TR\ OFF)}$ at the time of instantaneous break until the P_{XX} input voltage gets lower than V_{IL} (because release by reset is not available after the HALT mode is entered by instantaneous break).
- R5 and R6
  Make V^+ (V_{BE}≒0.6V is obtained by R5 and R6) when the reset circuit works (Tr ON) more than (operating V_{DD} min + V_F of diode D1).
  Observing this note, make V^+ as low as possible to provide a reset early enough after power-ON.
- Backup time
  The normal operation continues with a relatively high current dissipation from when power failure is detected by the P_{XX} until the HALT instruction is executed. Fix the C1 value so that the standby supply voltage is held during backup time of set + above-mentioned time.

2-1-5. Notes for software design

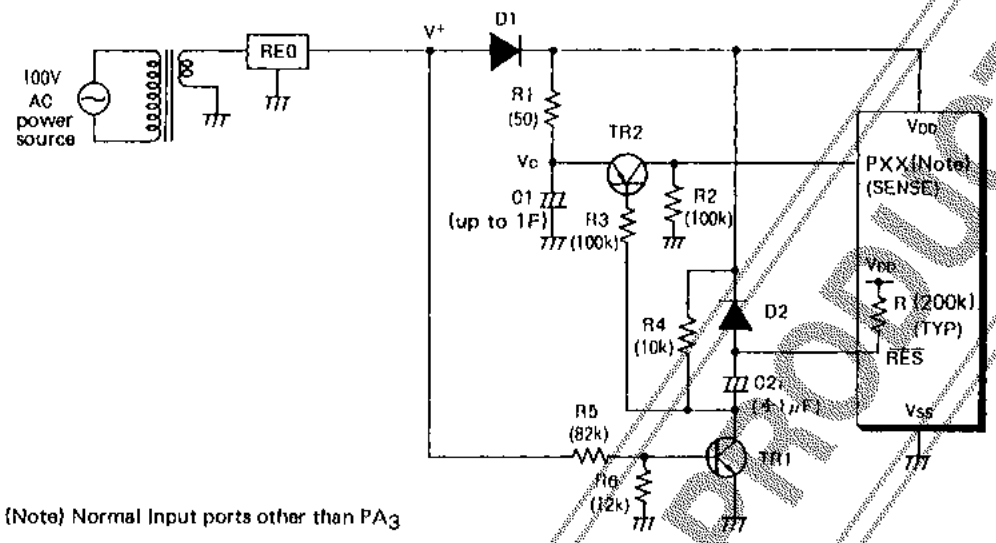
- Design the program so that port A_3 is brought to "H" level at the standby mode.
- Check a standby request by polling the input port twice.

(Example)

```
        :
        BP1     AAA     ; 1st polling
        BP1     AAA     ; 2nd polling
        HALT            ; Standby
        :
AAA:
```

2-2. Sample application 2 where the standby function is used for power failure backup
Shown below is a sample application where the program selects between power-ON reset and reset after power is restored.

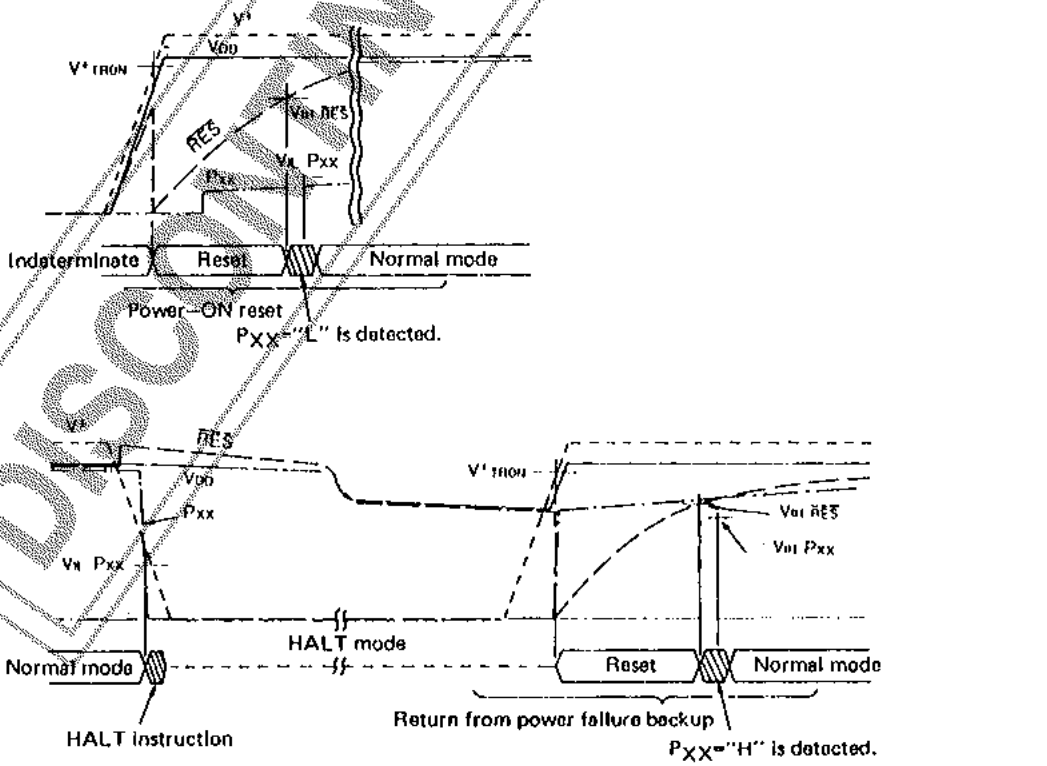
2-2-1. Sample application circuit – (2) (No instantaneous break in power source)
Fig. 2-3 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA_3

Fig. 2-3 Sample application – (2) where the standby function is used for power failure backup

2-2-2. Operating waveform in sample application circuit – (2)
The operating waveform in the sample application circuit in Fig. 2-3 is shown in Fig. 2-4. The mode is roughly divided as follows:
(1) Power-ON reset
(2) Return from power failure backup



V^+_{TRON}: V^+ value when TR1 is turned ON/OFF.

Fig. 2-4 Operating waveform in sample application circuit – (2)

2-2-3. Operation of sample application circuit – (2)

(a) At the time of power-ON reset

The operation and notes are the same as for sample application circuit – (1), except that after reset release P_{XX}="L" is program-detected to decide program start after initial reset.

(b) Standby initiation

When one polling regards the P_{XX} input voltage as "L" level, the HALT mode is entered.

(c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

After standby release P_{XX}="H" is program-detected, deciding program start after power is restored.

– Note –

If power is restored after V_{DD} during power failure backup gets lower than V_{IH} on the P_{XX}, P_{XX}="L" may be program-detected, deciding program start after initial reset.

2-2-4. Notes for design of sample application circuit – (2)

- R2 and R3

  Fix the R2 value so that R2≫R1 is yielded and fix the R3 value so that I_B of TR2 is limited.
- R4

  There is no severe restriction on the R4 value, but fix it so that C2 can discharge quickly.

  Other notes are the same as for sample application circuit – (1).

2-2-5. Notes for software design

- Dsign the program so that port A_3 is brought to "H" level at the standby mode.
- Check a standby request by polling the input port once.

(Example)

```
        ⋮
BP1     AAA     ; Polling
HALT            ; Standby
        ⋮
AAA:
```

2-3. Sample application 3 where the standby function is used for power failure backup

2-3-1. Sample application circuit – (3) (There is an instantaneous break in power source.)

Fig. 2-5 shows a sample application where the standby function is used for power failure backup.

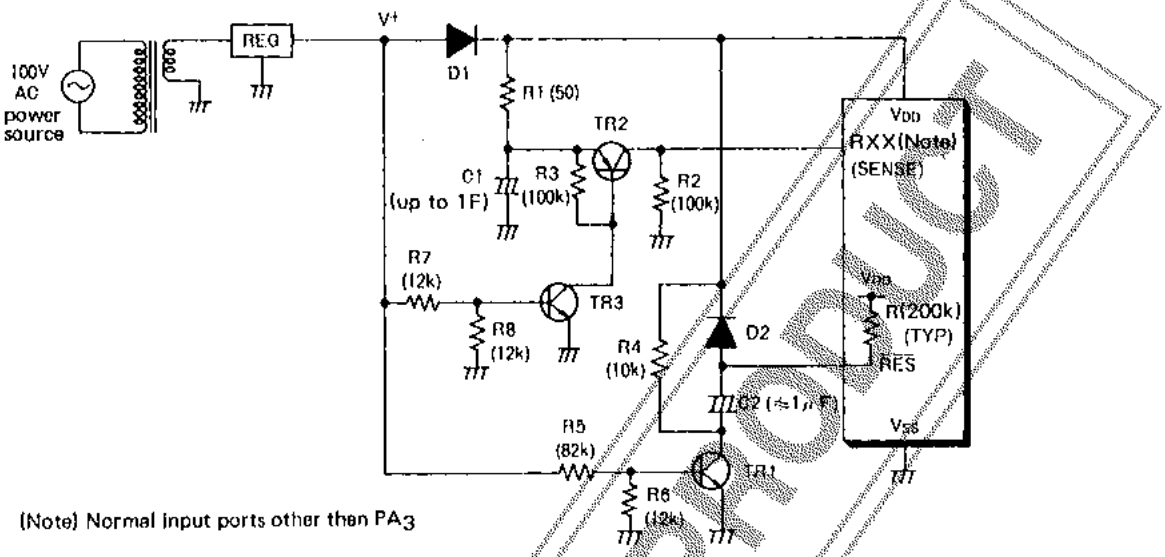


Fig. 2-5 Sample application – (3) where the standby function is used for power failure backup

2-3-2. Operating waveform in sample application circuit – (3)

The operating waveform in the sample application circuit in Fig. 2-5 is shown in Fig. 2-6. The mode is roughly divided as follows:

(1) Power-ON reset
(2) Instantaneous break of main power source
(3) Return from power failure backup

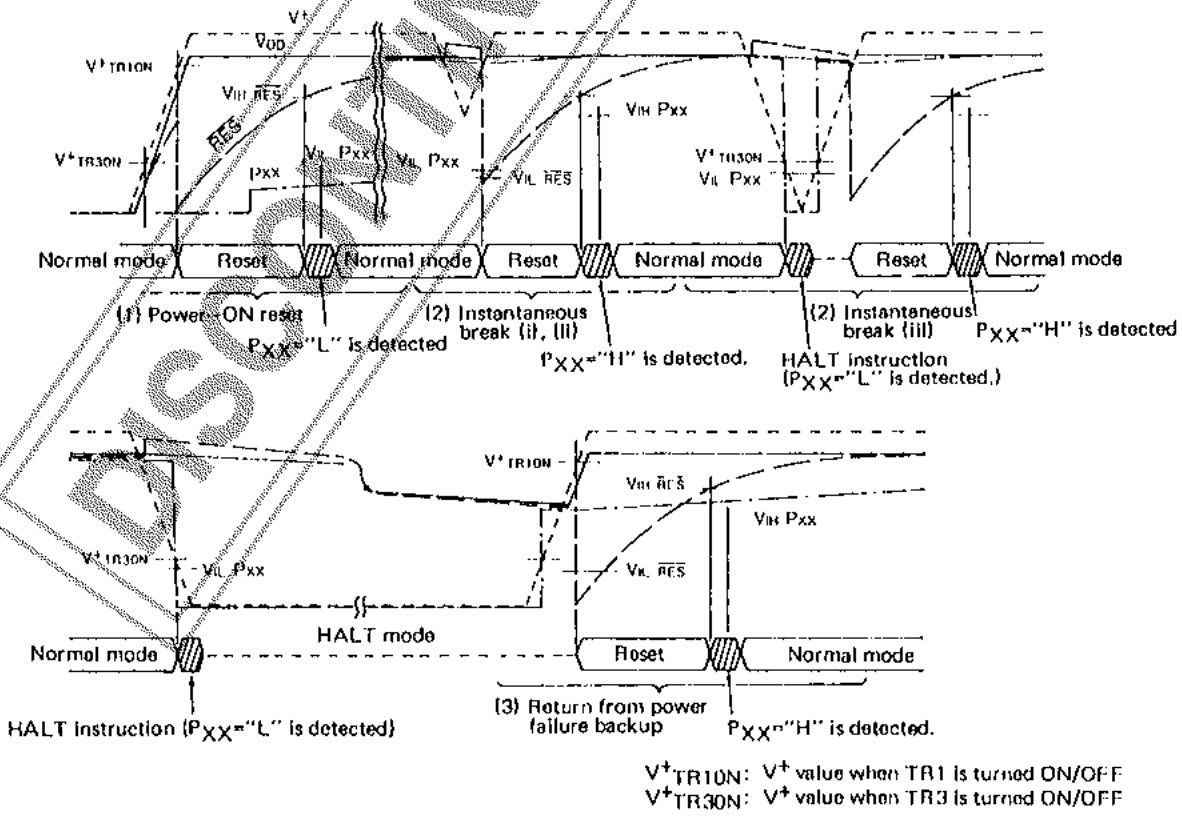


Fig. 2-6 Operating waveform in sample application circuit – (3)

2-3-3. Operation of sample application circuit – (3)

(a) At the time of power-ON reset
The operation and notes are the same as for sample application circuit – (2)

(b) At the time of instantaneous break

(i) When the P_{XX} input voltage does not meet V_{IL} (the P_{XX} input level does not get lower than input threshold level V_{IL}) and the $\overline{RES}$ input voltage only meets V_{IL}:
A reset occurs in the normal mode. After reset release P_{XX}="H" is program-detected, deciding program start after instantaneous break.

(ii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage meet V_{IL}:
When two pollings do not regard the P_{XX} input voltage as "L" level, the HALT mode is not entered and a reset occurs.
When two pollings regard the P_{XX} input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode. After standby release P_{XX}="H" is program-detected, deciding program start after instantaneous break.

(c) At the time of return from power failure backup
The operation and notes are the same as for sample application circuit – (2)

2-3-4. Notes for design of sample application circuit – (3)

- R3
  Bias resistance of TR2
- R7 and R8
  Fix the R7 and R8 values so that TR3 is turned ON/OFF at approximately 1.5V of V^+.

Other notes are the same as for sample application circuit – (1)

2-3-5. Notes for software design
Same as for sample application circuit – (1)