SANYO

LC7815

Monolithic C-MOS Integrated Circuit
2-Pole 4-Position Analog Function Switch

The LC7815 is a 2-pole 4-position analog function switch with 2 built-in C-MOS analog switches (LC4066 type). A soft touch of a button enables switchover of the input signal source of an audio amplifier.

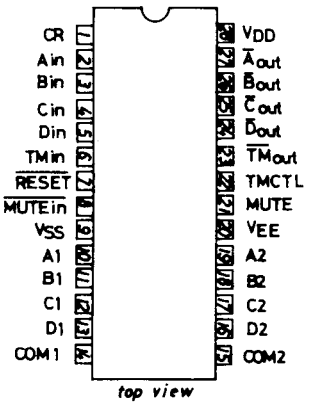
Use

Function switchover of amplifier, receiver, etc. (2 poles 4 positions)

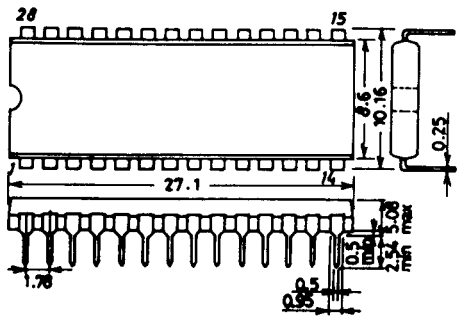
Features

1. Good distortion characteristic because of built-in analog switches of LC4066 type: Distortion 0.01 % max./ v_{in}=1Vrms, V_{DD}=15 to 18 V
2. Capable of outputting audio muting control signal to minimize noise to be generated at the time of switchover
3. Built-in controller for tape monitor switchover (using LC4066B together)
4. Built-in driver for LED which displays function mode, tape monitor mode
5. Since control input can be operated from + supply alone when using dual supplies, interface with other circuits can be achieved easily.
6. Since audio muting control signal can be triggered independently from external pin ($\overline{MUTE}_{in}$), audio muting at the time of return from backup can be achieved easily.
7. Control input pin ($\overline{RESET}$) to be used for turning OFF all analog switches
8. Backup can be performed easily because of C-MOS structure. (Backup voltage: 3 V min.)
9. Operating voltage: 4.5 to 18.0 V/single supply, $^{+4.5}_{-0}$ to ±9.0 V/dual supplies
10. Package: DIP-28 (Shrink type)

Pin Assignment



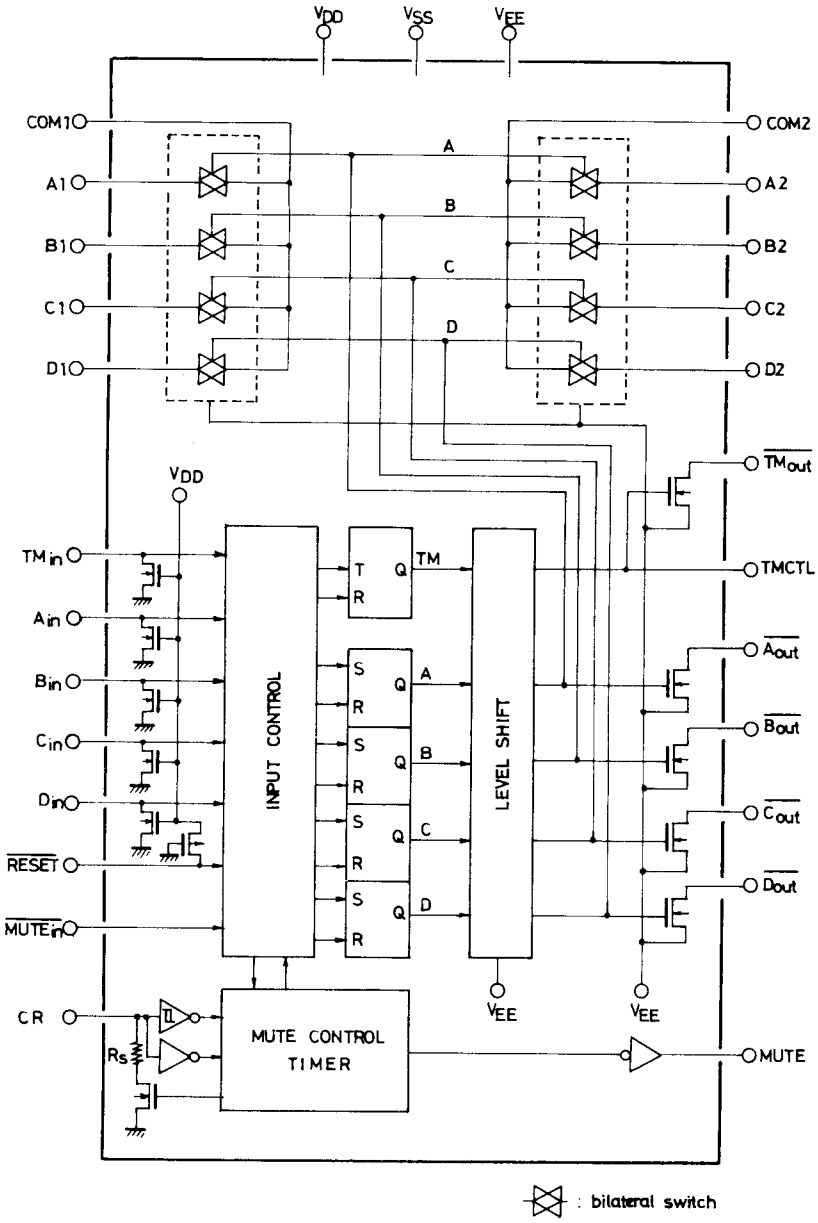
Case Outline 3029
(unit: mm)



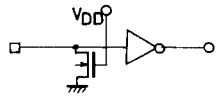
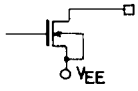
These specifications are subject to change without notice.

TOKYO SANYO ELECTRIC CO., LTD. SEMICONDUCTOR DIVISION
15-13, 6-CHOME, SOTOKANDA, CHIYODA-KU, TOKYO 101 JAPAN

Equivalent Circuit Block Diagram



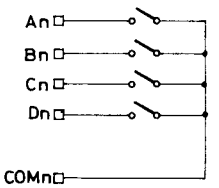
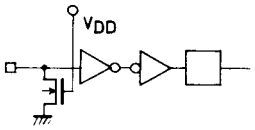
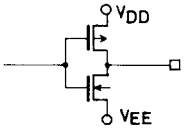
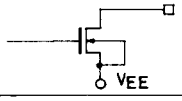
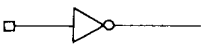
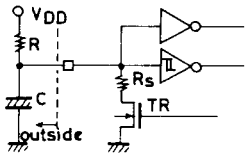
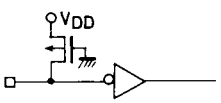
Pin Description

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Type of Input/Output</th><th>Pin Functions</th></tr>
<tr><td>V_{DD}
V_{SS}
V_{EE}</td><td>28
9
20</td><td></td><td>• Power supply pins
Single supply (+): $V_{SS}=V_{EE}=GND$
Dual supplies (+−): $V_{SS}=GND$, $V_{EE}=(-)V$</td></tr>
<tr><td>A_{in}, B_{in},
C_{in}, D_{in}</td><td>2, 3,
4, 5</td><td>  </td><td>• Specified input pins for turning ON individual analog switches
• Priority order of simultaneous push ($A_{in}>B_{in}>C_{in}>D_{in}$)
• Prevention of malfunction attributable to pulse noise (Pulse width is discriminated by muting delay time.)</td></tr>
<tr><td>$\overline{A}_{out}$,
$\overline{B}_{out}$,
$\overline{C}_{out}$,
$\overline{D}_{out}$</td><td>27,
26,
25,
24</td><td>  </td><td>• Output of driver for LED which displays ON state corresponding to individual analog switches
• N channel open drain (Source is connected to V_{EE}.)</td></tr>
<tr><td>A_1, B_1,
C_1, D_1

A_2, B_2,
C_2, D_2

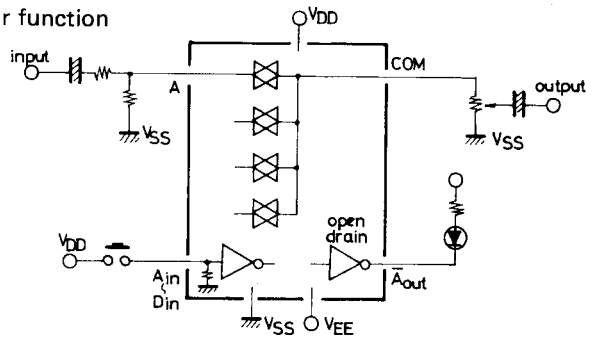
COM 1
COM 2</td><td>10, 11,
12, 13

19, 18,
17, 16

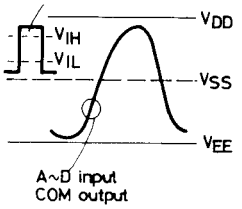
14
15</td><td>  </td><td>• A to D: Audio signal input pins
• COM: Audio signal output pins
• Signal inputs (A to D) conduct according to signal inputs (A_{in} to D_{in}) as follows:
<table><tr><th colspan="2">COM output</th><th>A_n</th><th>B_n</th><th>C_n</th><th>D_n</th></tr><tr><td rowspan="4">Specified input</td><td>A_{in}</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>B_{in}</td><td>*</td><td>1</td><td>0</td><td>0</td></tr><tr><td>C_{in}</td><td>*</td><td>*</td><td>1</td><td>0</td></tr><tr><td>D_{in}</td><td>*</td><td>*</td><td>*</td><td>1</td></tr></table>*: Don't care.</td></tr>
<tr><td>TM_{in}</td><td>6</td><td>  </td><td>• Input pin for specifying tape monitor mode ON/OFF
• Rise of input signal is detected; monitor mode ON/OFF are inverted to monitor mode OFF/ON respectively.</td></tr>
<tr><td>TMCTL</td><td>22</td><td>  </td><td>• Output pin for controlling external analog switch (LC4066B) for tape monitor
• Source of N channel transistor of complementary buffer output is connected to V_{EE}.</td></tr>
<tr><td>$\overline{TM}_{out}$</td><td>23</td><td>  </td><td>• Output pin for driver for LED which displays tape monitor state as well as external analog switch (LC4066B) for tape monitor
• TM_{out} is opposite in polarity to TMCTL.</td></tr>
<tr><td>$\overline{MUTE}_{in}$</td><td>8</td><td>  </td><td>◦ Input pin for forcing audio muting control signal (MUTE) to be triggered externally
◦ If fixed at 'L' level, MUTE output becomes 'H' level.</td></tr>
<tr><td>MUTE</td><td>21</td><td>  </td><td>• Output pin for audio muting control signal
◦ Signal with pulse width to be determined by external constant at CR pin is outputted at the time of function switchover or $\overline{MUTE}_{in}$ input.</td></tr>
<tr><td>CR</td><td>1</td><td>  </td><td>◦ CR time constant pin for determining time interval of audio muting control signal
• Time lag (muting delay) between muting signal rise and analog switch switchover depends on $C{\cdot}R_S$ time constant at the time of transistor ON.</td></tr>
<tr><td>$\overline{RESET}$</td><td>7</td><td>  </td><td>• Input pin for turning OFF all analog switches and resetting tape monitor flip-flop ('L' level active)</td></tr>
</table>

■ Application Circuits

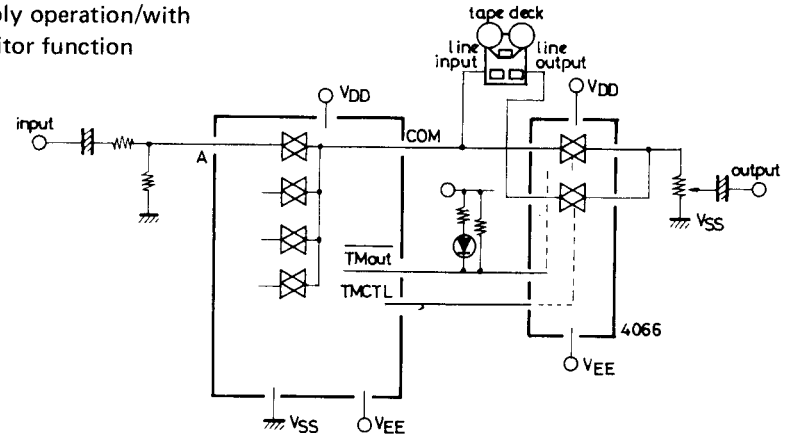
1. Dual-supply operation/without tape monitor function



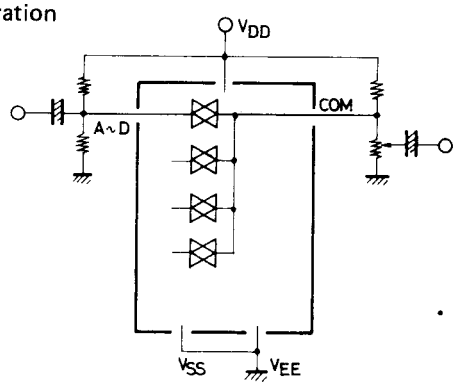
Control input

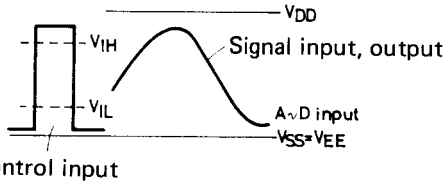


2. Dual-supply operation/with tape monitor function



3. Single-supply operation



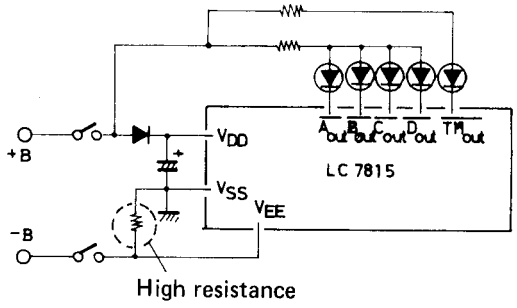


Control input

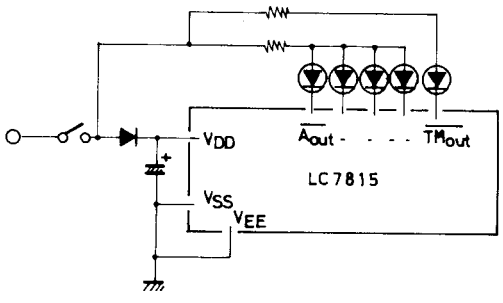
- For using tape monitor function, make connection as shown in 2 above.

4. Backup

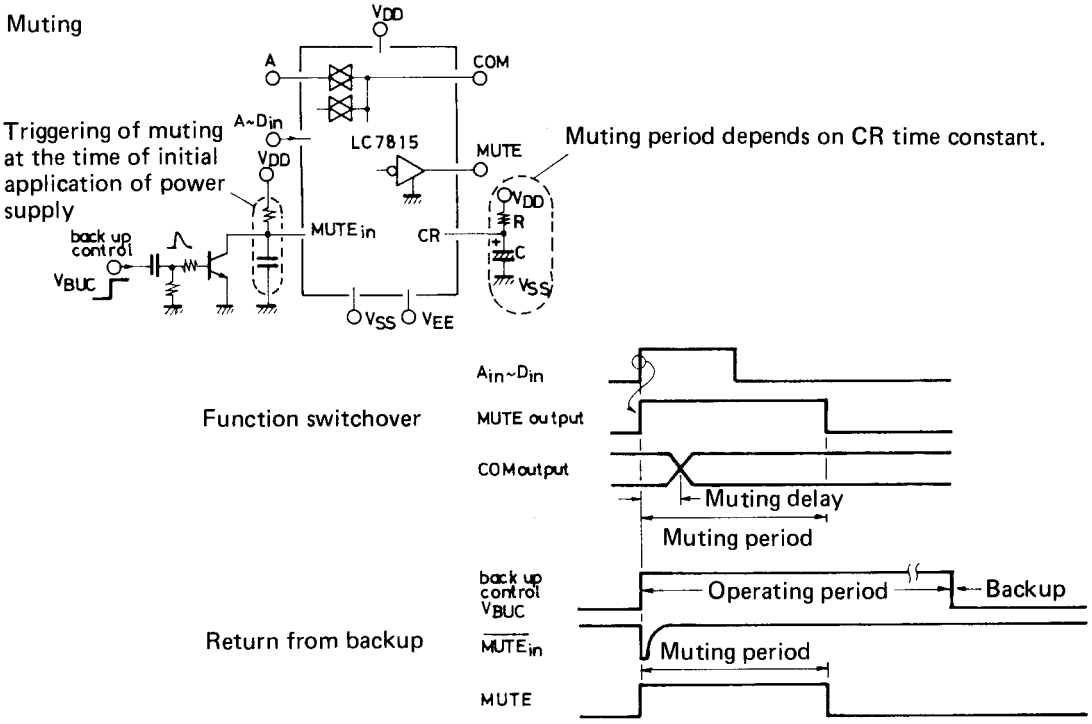
(1) Dual-supply operation



(2) Single-supply operation



5. Muting



Absolute Maximum Ratings/Ta=25 ±2°C

Maximum Supply Voltage	V_{DD}max		$V_{SS}-0.3\sim V_{EE}+20$	V
	V_{EE}max		$V_{DD}-20\sim V_{SS}+0.3$	V
Output Current	I_{OUT}	$\overline{A}_{out}$, $\overline{B}_{out}$, $\overline{C}_{out}$, $\overline{D}_{out}$, $\overline{TM}_{out}$	30	mA
Output Voltage	V_{OUT}	$\overline{A}_{out}$, $\overline{B}_{out}$, $\overline{C}_{out}$, $\overline{D}_{out}$, $\overline{TM}_{out}$	$V_{EE}-0.3\sim V_{DD}+0.3$	V
Voltage Difference at analog switch ON	ΔV_{on}	Switch ON	0.5	V
Allowable Power Dissipation	$P_d$max	Ta≦85°C	350	mW
Operating Temperature	T_{opg}		−40~+85	°C
Storage Temperature	T_{stg}		−40~+125	°C

Allowable Operating Ranges/Ta=−40~+85°C

Characteristic	Symbol	Pin No.	Conditions	min	typ	max	unit
Supply Voltage	V_{DD1}	V_{DD}(28)	$V_{EE}\leqq V_{SS}$	$V_{SS}+4.5$		$V_{EE}+18$	V
	V_{EE}	V_{EE}(20)	$V_{DD}\geqq V_{SS}+4.5$	$V_{DD}-18$		V_{SS}	V
	V_{DD2}	V_{DD}(28)	Backup $V_{EE}\leqq V_{SS}$	$V_{SS}+3$		$V_{SS}+18$	V
'H' Level Input Voltage	V_{IH1}	A_{in}(2)~D_{in}(5), $\overline{RESET}$(7), $\overline{MUTE}_{in}$(8)		0.75V_{DD}		V_{DD}	V
	V_{IH2}	TM_{in}(6)		0.8V_{DD}		V_{DD}	V
'L' Level Input Voltage	V_{IL1}	A_{in}(2)~D_{in}(5), $\overline{RESET}$(7), $\overline{MUTE}_{in}$(8)		V_{DD}		0.25V_{DD}	V
	V_{IL2}	TM_{in}(6)		V_{SS}		0.2V_{DD}	V
Analog Switch Input Voltage	V_{IN}	A_1(10)~D_1(13), A_2(19)~D_2(16)		V_{EE}		V_{DD}	V
External Capacitance for Muting Timer	C	CR(1)				10	μF
External Resistance for Muting Timer	R	CR(1)	$V_{DD}-V_{SS}$=4.5V			100	kΩ
			$V_{DD}-V_{SS}\geqq$9V			300	kΩ
Input Receiving Pulse Width	T_{IN}	A_{in}(2)~D_{in}(5), TM_{in}(6)	V_{DD}=9V, C=3.3μF, R=220kΩ	120			ms

Electrical Characteristics/Ta=25 ±2°C, V_{SS}=0V

Characteristic	Symbol	Pin No.	Conditions	min	typ	max	unit
'H' Level Output Voltage	V_{OH1}	TMCTL(22)	I_{OH}=−0.1mA V_{DD}=4.5~18V	0.8V_{DD}		V_{DD}	V
	V_{OH2}	MUTE(21)	I_{OH}=−0.4mA, V_{DD}=4.5V	V_{DD}−1.5		V_{DD}	V
			I_{OH}=−0.4mA, V_{DD}=9V	V_{DD}−0.5		V_{DD}	V
'L' Level Output Voltage	V_{OL1}	TMCTL(22)	I_{OL}=0.1mA	V_{EE}		0.2X (V_{DD}−V_{EE})	V
	V_{OL2}	MUTE(21)	I_{OL}=0.4mA, V_{DD}=4.5V	0		1.5	V
			I_{OL}=0.4mA, V_{DD}=9V	0		0.5	V
	VOL3	$\overline{A}_{out}$(27), $\overline{B}_{out}$(26), $\overline{C}_{out}$(25), $\overline{D}_{out}$(24),	I_{OL}=7mA, V_{DD}−V_{EE}=4.5V	VEE		V_{EE}+2	V
		$\overline{TM}_{out}$(23)	I_{OL}=30mA, V_{DD}−V_{EE}=9V	V_{EE}		V_{EE}+4	V
			I_{OL}=30mA, V_{DD}−V_{EE}=18V	V_{EE}		V_{EE}+2	V
Analog Switch ON Resistance	R_{on}	A_1(10), B_1(11),	I=1mA, V_{DD}−V_{EE}=4.5V		400		Ω
		C_1(12), D_1(13),	I=1mA, V_{DD}−V_{EE}=9V		120		Ω
		COM1(14), A_2(19), B_2(18), C_2(17), D_2(16) COM2(15)	I=1mA, V_{DD}−V_{EE}=18V		80		Ω
'H' Level Input Current	I_{IH1}	A_{in}(2), B_{in}(3), C_{in}(4), D_{in}(5), TM_{in}(6)	V_{DD}=9V, V_{IN}=V_{DD}	20		90	μA
	I_{IH2}	$\overline{MUTE}_{in}$(8)	V_{IN}=V_{DD}=18V			10	μA
'L' Level Input Current	I_{IL1}	$\overline{RESET}$(7)	V_{DD}=9V, V_{IN}=V_{DD}	−90		−20	μA
	I_{IL2}	$\overline{MUTE}_{in}$(8)	V_{IN}=V_{SS}	−10			μA
Input/Output OFF Leak Current	I_{OFF1}	$\overline{A}_{out}$(27)~$\overline{D}_{out}$(24) $\overline{TM}_{out}$(23)	Output transistor OFF Vo=V_{EE}+18V			10	μA
	I_{OFF2}	CR(1)	Output transistor OFF Vo=V_{SS}+18V			3	μA
	I_{OFF3}	A_1(10),~D_1(13), COM1(14), A2(19)~D_2(16), COM2(15)	Analog switch OFF V_{IN}=Vo=V_{EE}~18V	−10		10	μA
Input Floating Voltage	V_{IF1}	A_{in}(2)~D_{in}(5), TM_{in}(6)	V_{DD}=4.5~18V			0.75	V
	V_{IF2}	$\overline{RESET}$(7)	V_{DD}=4.5~18V	V_{DD}−0.75			V
Total Harmonic Distortion	THD_1	COM1(14), COM2(15)	V_{IN}=1Vrms, f=1kHz, V_{DD}−V_{EE} =15~18V, Refer to Fig. 1.			0.01	%
	THD_2	COM1(14), COM2(15)	V_{IN}=0.1Vrms, f=1kHz, V_{DD} −V_{EE}=4.5V, Refer to Fig. 1.			0.05	%
Feedthrough (Switch OFF)	FTH	A_1(10), D_1(13) to COM1(14)	V_{DD}−VEE=18V, F=10kHz V_{in}=0.77Vrms, Refer to Fig. 2. R_L=47kΩ	55			dB
		A_2(19), D_2(16) to COM2(15)					
Crosstalk	CT	A_1(10), D_1(13) to COM2(1)	V_{DD}−V_{EE}=18V, f=10kHz V_{in}=0.7Vrms, Refer to Fig. 3. R_L=47kΩ	75			dB
		A_2(19), D_2(16) to COM1(14)					
Muting period	T_{M1}	MUTE(21)	V_{DD}=9V, Refer to Fig. 4. C=3.3μF ±20%, R=220kΩ ±5%	350	580	1000	ms
	T_{M2}	MUTE(21)	V_{DD}=9V, C=3.3μF ±0%, R=220kΩ ±0%	450	580	800	ms

Switch Switchover Delay Time	T_{SWD}	$A_{in}(2)\sim D_{in}(5)$, $TM_{in}(6)$	V_{DD}=9V, Refer to Fig. 5. C=3.3μF, R=220kΩ	30	50	120	ms
Supply Current	I_{DD1}	$V_{DD}(28)$	Operating, Refer to Fig. 6. $V_{DD}-V_{EE}$=18V			1000	μA
	I_{DD2}	$V_{DD}(28)$	Backup, V_{DD}=5V, V_{SS}=V_{SS}			3	μA

Fig. 1 Total harmonic distortion

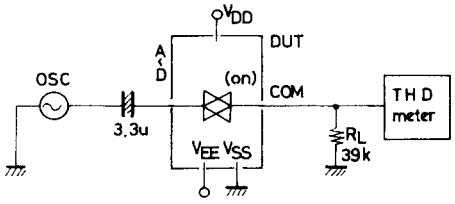
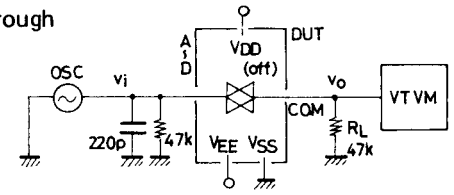
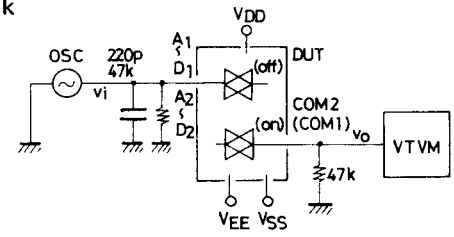


Fig. 2 Feedthrough



$$FTH = 20 \log \frac{V_O}{V_i} \quad (dB)$$
v_i = 770mVrms
$V_{DD} - V_{EE}$ = 18V

Fig. 3 Crosstalk



$$CT = 20 \log \frac{V_O}{V_i} \quad (dB)$$
v_i = 770mVrms
$V_{DD} - V_{EE}$ = 18V

Fig. 4 Muting period

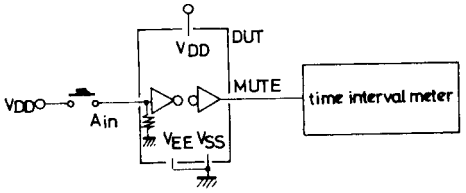


Fig. 6 Supply current

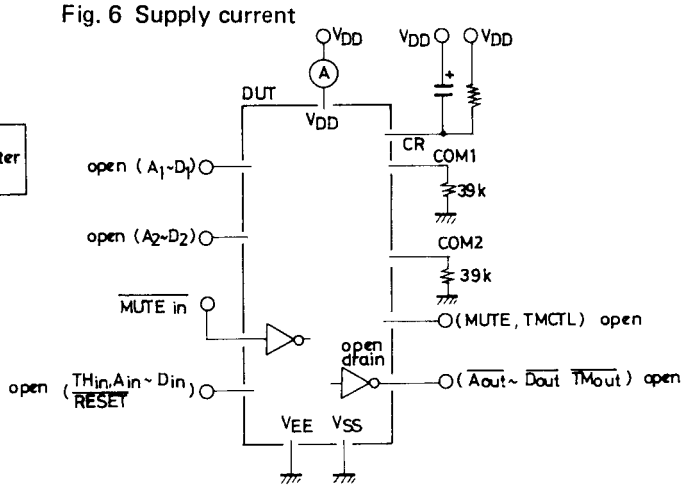
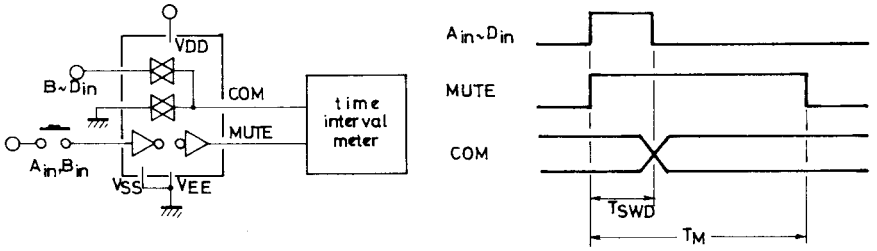


Fig. 5 Switch switchover delay time



T_M: Muting period
T_{SWD}: Switch switchover delay time