

M51397AP

SECAM CHROMA SYSTEM

DESCRIPTION

The M51397AP is a semiconductor integrated circuit for SECAM system color television receivers. It CONTAINS chroma processor, chroma demodulator, DC regenerator and system switches for PAL/SECAM dual system. Dual system color television receivers can be implemented by M51395AP (PAL chroma system and video processor) and M51397AP (SECAM chroma processor and system switch).

FEATURES

- Automatic mode switching for dual systems.
- Common delay line for dual systems.
- Minimum external components.
- Directly drives chroma output transistors.

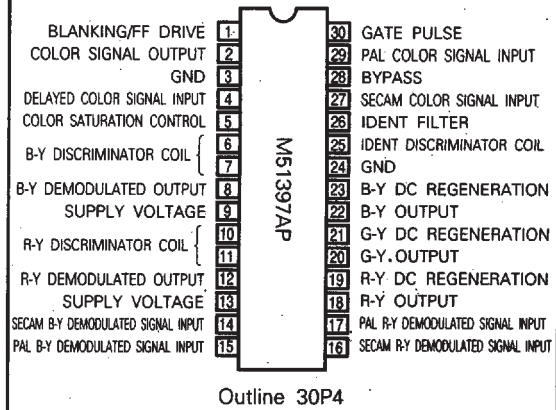
APPLICATION

SECAM system color TV, color signal processors

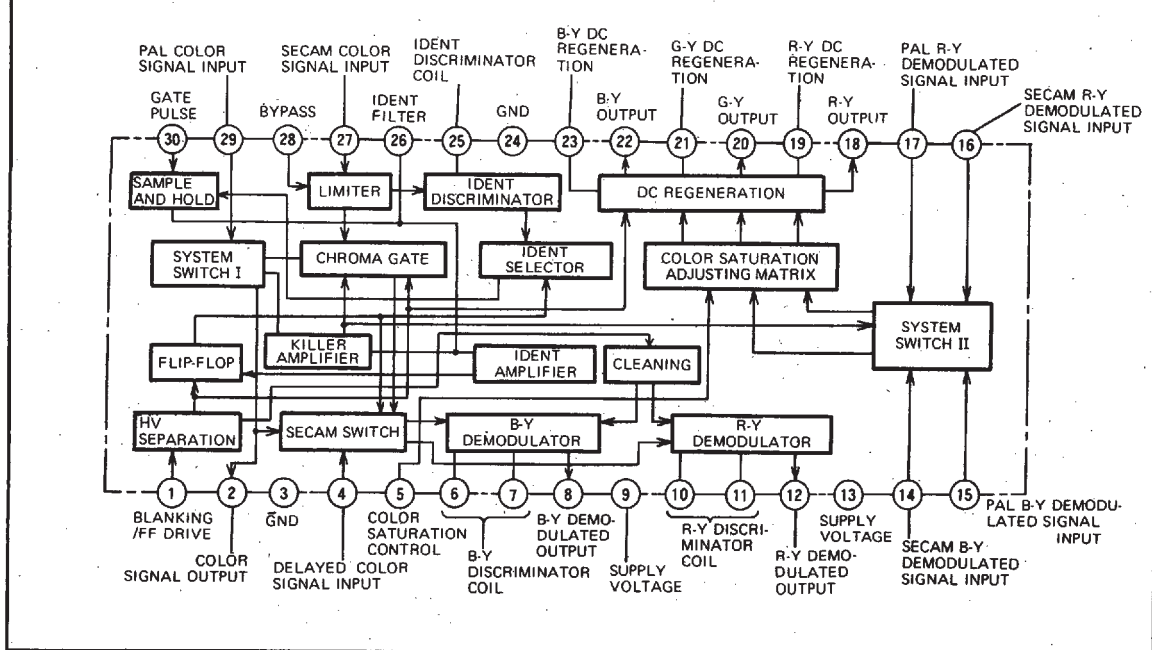
RECOMMENDED OPERATING CONDITION

Supply voltage range 11~13V
 Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V _{CC}	Supply voltage	16.0	V
P _d	Power dissipation	1400	mW
T _{opr}	Operating temperature	-20~65	°C
T _{stg}	Storage temperature	-40~125	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C, unless otherwise noted)

Symbol	Parameter	Input signal	Conditions		Meas. point	Limits			Unit	Note		
			Input	V _s		Min.	Typ.	Max.				
V _{CC}	Supply voltage	SG1	27	6	9, 13	10	12	14	V	—		
I _{CC}	Circuit current	SG1	27	6	a	55	75	88	mA	—		
V _{OLIM}	Limiting output level	SG2	27	—	2	1.9	2.2	2.7	V _{P-P}	1		
G _{LIM}	Gain of limiter					28	32	36	dB	2		
V _{OSS}	Output level of SECAM SW	SG1	27	—	6, 10	1.4	1.7	2.0	V _{P-P}	—		
G _{SW}	Gain of SECAM SW limiter	SG2	4	—		.12	18	24	dB	3		
V _{ODIS}	Output level of ident Disc.	SG2	27	—	25	0.48	0.59	0.70	V _{P-P}	4		
V _{IK}	Ident killer threshold level			6	20	38	48	58	dB	5		
V _{OK}	Killed output level	SG1	27	8	18, 20 22	—	5	20	mV _{P-P}	6		
E _{OB-Y}	Demodulated output level	B-Y	SG1	27	—	b, c	0.86	0.98	1.13	V _{P-P}	7	
E _{OR-Y}		R-Y					0.58	0.68	0.78			
$\frac{E_{OR-Y}}{E_{OB-Y}}$	Ratio of dem. output R-Y/B-Y	R-Y/ B-Y					0.60	0.70	0.80	—	8	
Lin I	Linearity of dem. output	I	SG2	27	—	b, c	2.4	2.8	3.2	—	9	
Lin II		II					2.2	2.6	3.0			
ΔE _{OIH}	Offset voltage of SECAM-SW	OFF	—	—	b, c	—	5	20	mV	10		
ΔE _{O/IN}	Offset voltage vs input level	SG2	27	—	b, c	—	4	10	mV	11		
AMR	AMR	SG2	27	—		—	-30	-25	dB	12		
V _{COL}	Color control voltage	OFF	—	—	5	5.6	6.0	6.4	V _{DC}	13		
V _{SAT min}	Color saturation control	MIN	SG1	27	—	18, 20 22	5	—	-20	dB	14	
V _{SAT grad}		GRAD					5.78	-9.7	-5.7			-1.7
V _{SAT max}		MAX					7	1.6	4.1			6.6
V _{SAT nor}		NOR					5.88	2.8	4.0			5.6
V _{OB-Y max}	Maximum non distortion output voltage	B-Y	SG1	27	—	22	4.1	5.1	—	V _{P-P}	15	
V _{OR-Y max}		R-Y					18	3.0	3.8			—
V _{OG-Y max}		G-Y					20	1.8	2.3			—
V _{B-Y/R-Y}	Output ratio of matrix	$\frac{(B-Y)}{(R-Y)}$	SG1	27	—	22, 18 20, 18	115	130	145	%	16	
V _{G-Y/R-Y}		$\frac{(G-Y)}{(R-Y)}$					52	60	68			
V ₁₈	Demodulated output DC voltage		SG1	27	4	18 20 22	6.6	7.2	7.8	V _{DC}	17	
V ₂₀												
V ₂₂												
ΔV ₁₈₋₂₀	Offset voltage among output terminals		SG1	27	4	18 20 22	-0.1	0	0.1	V _{DC}	18	
ΔV ₂₀₋₂₂												
ΔV ₂₂₋₁₈												
V _{CR B-Y}	Cross talk of system SW (PAL-SECAM)	I	SG3	14, 16 15, 17	6	22, 18	—	40	100	mV _{P-P}	19	
V _{CR R-Y}		II										
V _{OB-Y min}	Output voltage at minimum color control	I	SG3	14, 16 15, 17	4	18, 20 22	—	20	50	mV _{P-P}	20	
V _{OR-Y min}		II										
E _{CR B-Y}	Cross talk of demodulator	B-Y	SG1	27	8	22 18	33	38	—	dB	21	
E _{CR R-Y}		R-Y										

SECAM CHROMA SYSTEM

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Input signal	Conditions		Meas. point	Limits			Unit	Note		
			Input	V _s		Min.	Typ.	Max.				
V ₄	DC voltage at SECAM SW ④	I	OFF	—	—	4	2.2	2.8	3.4	V _{DC}	22	
V _{4 min}		II					—	0	0.5			
ΔE _{O I}	Offset voltage of demodulated voltage between each H	I	SG1	27	—	b, c	—	10	20	mV _{DC}	23	
ΔE _{O II}		II	SG2	27, 4			—	20	50			
ΔV _{OR-Y/H}	Offset voltage of output between each H		SG1	27	6		18	—	20	30	mV _{DC}	24
ΔV _{OB-Y/H}							22					
ΔV _{R-Y/COL}	DC offset voltage vs color control		OFF	—	—		18	-30	0	30	mV _{DC}	25
ΔV _{G-Y/COL}							20					
ΔV _{B-Y/COL}							22					
ΔV _{B-R/COL}	DC offset voltage among outputs vs color control		OFF	—	—		18	-30	0	30	mV _{DC}	26
ΔV _{R-G/COL}							20					
ΔV _{G-B/COL}							22					
V _{OR-YSII}	Output voltage of system SW II/DC-clamp	I	SG3	14, 16	8		18	2.1	2.6	3.1	V _{P-P}	27
V _{OB-YSII}		II		15, 17			22					
V _{OS I}	Output voltage of system SW I		SG2	29	—		2	1.5	1.9	2.3	V _{P-P}	30
ΔE _{OCR I}	Crosstalk of system SW I	I	SG2	27	—		2	—	40	100	mV _{P-P}	31
ΔE _{OCR II}		II		29			—	70	150			
ΔE _{OB-Y/V_{CC}}	Change of demodulated output vs V		SG1	27	—		b	0.06	0.09	0.12	1/V	28
ΔE _{OR-Y/V_{CC}}							c					
ΔE _{OB-Y/T_a}	Change of demodulated output vs T		SG1	27	—		b	-2	0	2	mV/°C	29
ΔE _{OR-Y/T_a}							c					
ΔV _{OR-Y/V_{CC}}	Change of output voltage vs V		SG1	27	8		18	0.09	0.13	0.16	1/V	28
ΔV _{OG-Y/V_{CC}}							20					
ΔV _{OB-Y/V_{CC}}							22					
ΔV _{OR-Y/T_a}	Change of output voltage vs T		SG1	27	8		18	-30	0	30	mV/°C	29
ΔV _{OG-Y/T_a}							20					
ΔV _{OB-Y/T_a}							22					
ΔV _{OB-R/V_{CC}}	Offset voltage among output terminals vs V		OFF	—	—		18	-25	0	25	mV/V	32
ΔV _{OR-G/V_{CC}}							20					
ΔV _{OG-B/V_{CC}}							22					
ΔV _{OB-R/T_a}	Offset voltage among output terminals vs T		OFF	—	—		18	-1	0	1	mV/°C	29
ΔV _{OR-G/T_a}							20					
ΔV _{OG-B/T_a}							22					

Symbol	Parameter	Meas. point	Limits			Unit
			Min.	Typ.	Max.	
V _{G on}	Gate pulse	On level	1.4	—	—	V _{O-P}
V _{G off}		Off level	—	—	0.5	
V _{BLK on}	Blanking pulse	On level	6.8	—	—	V _{O-P}
V _{BLK off}		Off level	—	—	5.6	
V _{FF on}	F.F. drive pulse	On level	10.8	—	—	V _{O-P}
V _{FF off}		Off level	—	—	8.9	
V _{i max}	Maximum chroma input signal at limiter	27	—	—	3.0	V _{P-P}
V _{i dly}	Input signal level at delayed input of SECAM SW	4	0.6	0.8	1.2	V _{P-P}
V _{ISS max}	Maximum input level of system SW	14-17	—	—	1.2	V _{P-P}

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test terminal	Limits			Unit
			Min.	Typ.	Max.	
Ri (SEC)	SECAM Chroma input resistance	Pin 27	—	2.5	—	k Ω
Ci (SEC)	SECAM Chroma input capacitance	Pin 27	—	1.6	—	pF
Ri (PAL)	PAL Chroma input resistance	Pin 29	—	3.0	—	k Ω
Ro (C)	Chroma output resistance	Pin 2 RL=1.2k Ω	—	20	—	Ω
Ri (SW)	SECAM Switch input resistance	Pin 4	—	2.0	—	k Ω
Ci (SW)	SECAM Switch input capacitance	Pin 4	—	3.5	—	pF
Ro (DISC)	SECAM SW Output impedance	Pins 6, 10	—	200	—	Ω
Ri (DISC)	Discriminator input resistance	Pins 7, 11	—	1.8	—	k Ω
Ci (DISC)	Discriminator input capacitance	Pins 7, 11	—	3.0	—	pF
Ro (DISC)	Discriminator output resistance	Pins 8, 12	—	300	—	Ω
Ri (SYS)	System switch input resistance	Pins 14, 15, 16, 17	—	4.0	—	k Ω
Ro (REG)	Demodulator output resistance	Pins 18, 20, 22	—	300	—	Ω

ELECTRICAL CHARACTERISTICS TEST METHOD

- Note:1 V_{e} (@SW3 → ON. Input signal
f=4.3MHz, $V_{\text{e}}=100\text{mV}_{\text{P-P}}$)
- Note:2 $20\log (V_{\text{e}-1}/V_{\text{e}-2})$, where $V_{\text{e}-1}$ (100mV_{P-P})
→ $V_{\text{e}-2}$ (@ $V_{\text{e}} \rightarrow 0$), f=4.3MHz
- Note:3 Same as Note 2 (input $V_{\text{e}-1}$, 1V_{P-P}, f=4.3MHz)
- Note:4 Input signal f=4.328MHz, 200mV_{P-P}
- Note:5 $20\log (V_{\text{e}-1}/V_{\text{e}-2})$ where $V_{\text{e}-1}$ (100mV_{P-P})
→ $V_{\text{e}-2}$ (@ $V_{\text{e}} \rightarrow 0$)
- Note:6 Measured after eliminating SYNC pulses.
- Note:7 Center Value of carrier @SW2 → b,c
- Note:8 $V_{\text{b}}/V_{\text{c}}$
- Note:9 Output linearity (I) = $\frac{(V_{\text{o}} \text{ at } f_{\text{o}} + 300\text{kHz}) - (V_{\text{o}} \text{ at } f_{\text{o}})}{(V_{\text{o}} \text{ at } f_{\text{o}} + 100\text{kHz}) - (V_{\text{o}} \text{ at } f_{\text{o}})}$
Output linearity (II) = $\frac{(V_{\text{o}} \text{ at } f_{\text{o}} - 300\text{kHz}) - (V_{\text{o}} \text{ at } f_{\text{o}})}{(V_{\text{o}} \text{ at } f_{\text{o}} - 100\text{kHz}) - (V_{\text{o}} \text{ at } f_{\text{o}})}$
SW2 → d, e, SW3 → ON; 2200pF at b, c
Reference Signal at b: 4.406MHz (f_{OR}), 200mV_{P-P}
Reference Signal at c: 4.25MHz (f_{OS}), 200mV_{P-P}
- Note:10 V_{o} at 1H, (SW2 → d, e, SW3 → ON, SW4 → ON,
SW5 → ON)
- Note:11 ΔV_{o} at 20dB change of input signal
SW2 → d, e, SW3 → ON, SW4 → ON, SW5 → ON
Reference signal at b: 4.406MHz, 200mV_{P-P}
Reference signal at c: 4.25MHz, 200mV_{P-P}
DC Voltage between blanking interval and signal
interval are adjusted to same voltage by L₁, L₂
- Note:12 $20\log V_{\text{A}}/V_{\text{F}}$ (db)
SW2 → d, e, SW3 → ON, Input signal voltage
200mV_{P-P} without SYNC
Output voltage V_F: SG2 4.25MHz, 4.406MHz FM
modulated by f_m=400Hz, 75kHz
Output voltage V_A: SG2 4.25MHz, 4.406MHz AM
modulated by f_m=400Hz, 30%

Note:13 V_{e} at No Load.

Note:14 $\frac{V_{\text{o}} \text{ at } V_{\text{e}}}{V_{\text{o}} \text{ at } V_{\text{e}}=6\text{V}}$ (dB) (SW2 → b, c, SW6 → k, l)

Note:15 Maximum Output Voltage without distortion at a
change of V_{e}

Note:16 $\frac{V_{\text{o}} \text{ (B-Y)} V_{\text{o}} \text{ (G-Y)}}{V_{\text{o}} \text{ (R-Y)} V_{\text{o}} \text{ (R-Y)}}$ ($V_{\text{o}} \text{ (R-Y)}=2V_{\text{P-P}}$)

Note:17 DC voltage at $V_{\text{e}}=4\text{V}$

Note:18 $V_{\text{e}}-V_{\text{e}}$, $V_{\text{e}}-V_{\text{e}}$, $V_{\text{e}}-V_{\text{e}}$ (at $V_{\text{e}}=4\text{V}$)

Note:19 SG3=0.4V_{P-P}, 500kHz $V_{\text{e}}=6\text{V}$ SW2→d, e

I (Crosstalk SECAM → PAL)

Each output level at SW5→ON, SW6→k, l

II (Crosstalk PAL → SECAM)

Each output level at SW3→ON, SW5→OFF, SW6→m,n

Note:20. Same measurement as Note:23 at $V_{\text{e}} = 4\text{V}$

Note:21 Ratio of output voltage between each line (dB),
at SW2 → d, e, SW4 → ON

Note:22 I V_{e} DC at SW3 → ON

II V_{e} DC at SW5 → ON

Note:23 I Difference of output level between each line at
SW2 → d, e

II Difference of output level between each line at
SW1 → 2 SW2 → d, e, $V_{\text{e}} \rightarrow 1V_{\text{P-P}}$

Frequency at pin 27 and 4 are same (4.25 and
4.406MHz)

$V_{\text{e}} 1V_{\text{P-P}}+3\text{dB} \sim 1V_{\text{P-P}}-3\text{dB}$

Note:24 Difference of output level between each line at
SW2 → b, c, SW6 → k, l

Note:25 Difference of DC output voltage between as the
change of color control

Note:26 Difference of DC output voltage between each
output as the change of color control

Note:27 Output level at SG 0.4 V_{P-P}, 500kHz, SW2 de, color
VR max

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I SW3 → ON, SW6 → k, I

II SW3 → OFF, SW6 → m, n

Note:28 $V_{10} - V_{12} / 4 - V_{14}$

where V_{10} , V_{12} , V_{14} are output voltages at supply voltage 10, 12, 14V.

Note:29 Topg-20 ~ +65°C.

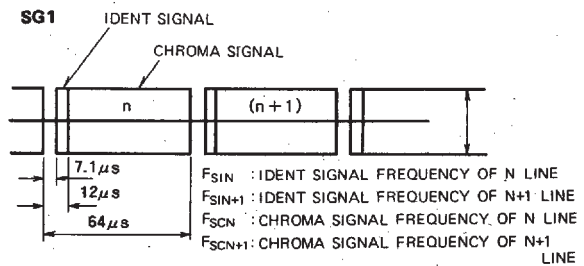
Note:30 Output level (after eliminating SYNC pulse) at input Signal 2 V_{P-P} , $f=4.3\text{MHz}$

Note:31 I (Crosstalk SECAM → PAL) Input Signal at ②
100mV_{P-P}, $f=4.3\text{MHz}$, without SYNC pulse

II (Crosstalk PAL → SECAM) Input Signal at ③
2V_{P-P}, $f=4.3\text{MHz}$, SW3 → ON, SW5 → ON without SYNC pulse

Note:32 Change of output voltage via supply voltage 10, 12, 14 volts (mV/V).

INPUT SIGNAL



REFERENCE LEVEL 0dB : $e_c = 100\text{mV}_{P-P}$

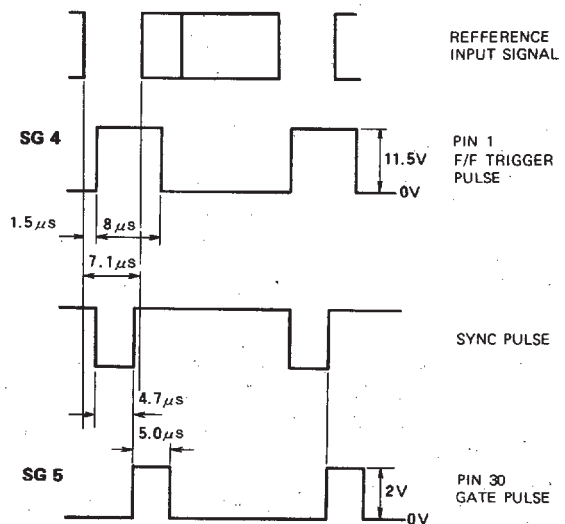
FREQUENCY OF SG1

Symbol	n line	n+1, line
f_{s1}	4.250	4.406
$W = f_0$	4.250	4.406
Y	4.020	4.3605
CY	4.3276	4.686
G	4.0976	4.6345
MG	4.4024	4.1715
R	4.1724	4.126
B	4.480	4.4515
BK	4.250	4.406

SG2 4.3 ± 0.5 MHz SINE WAVE

SG3 100K ~ 2 MHz SINE WAVE

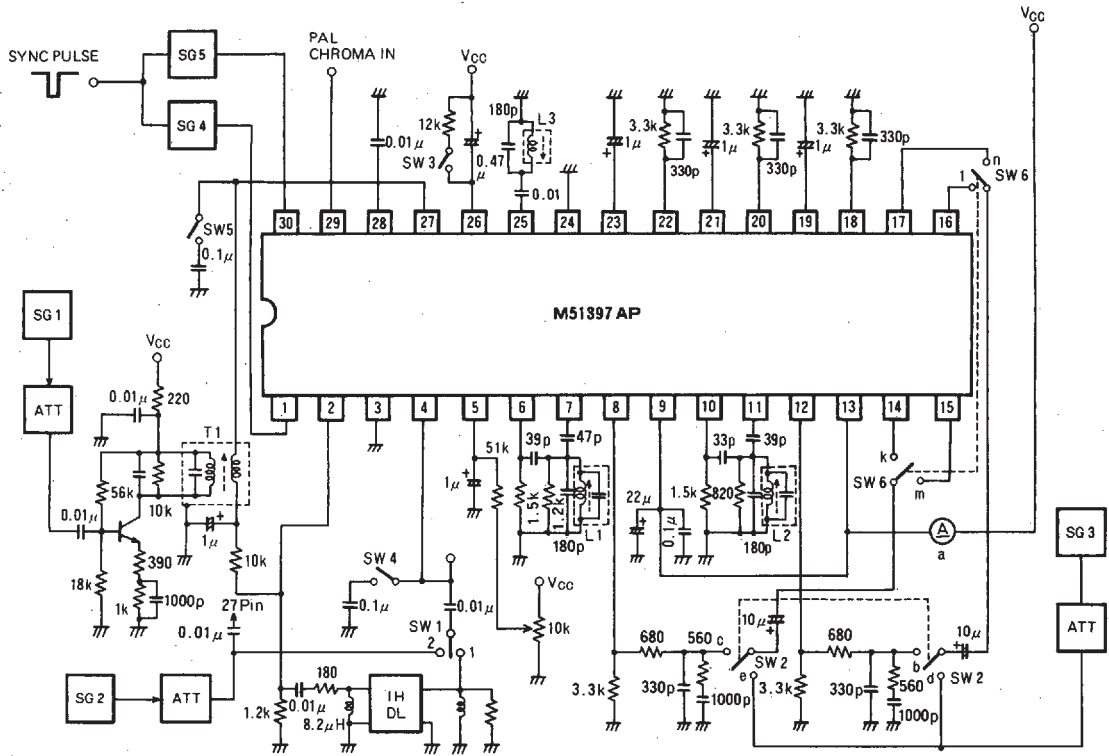
Gate Pulse & F/F Trg. Pulse



M51397AP

SECAM CHROMA SYSTEM

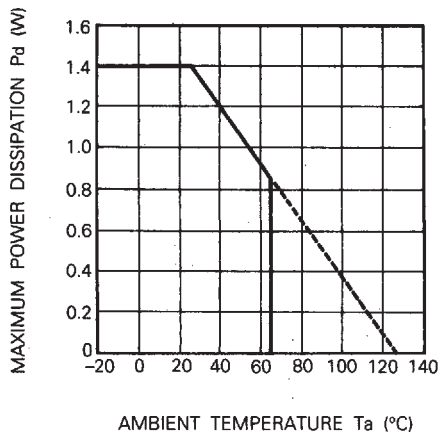
TEST CIRCUIT



Units Resistance: Ω
Capacitance: F

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

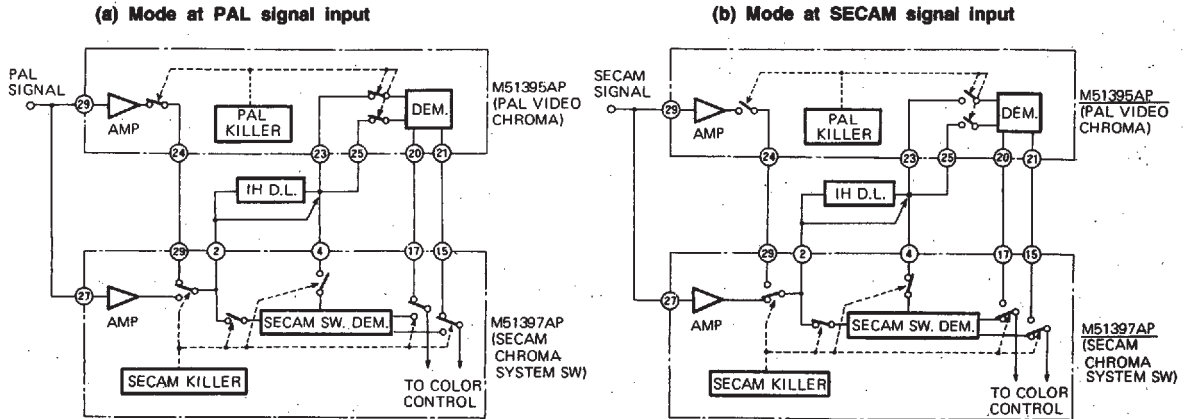


M51397AP

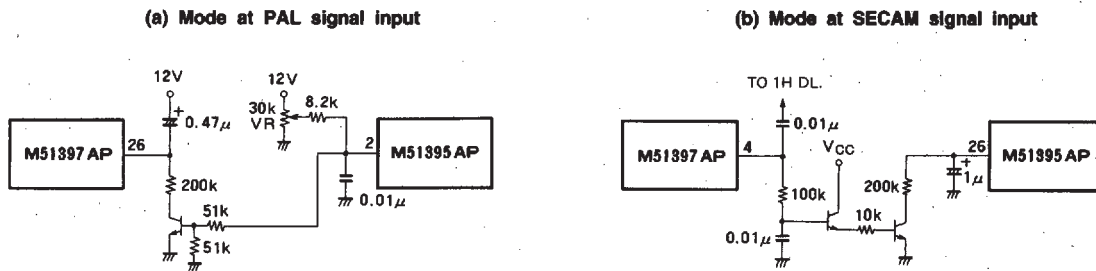
SECAM CHROMA SYSTEM

APPLICATION EXAMPLE OF M51395AP, M51397AP FOR PAL SECAM DUAL SYSTEM

MODE OF SYSTEM SW



APPLICATION EXAMPLE FOR CONTROL OF THE PRIORITY OF THE DUAL MODE



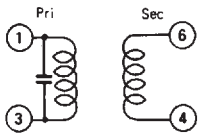
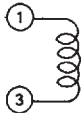
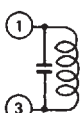
M51395AP (When the M51395AP is applied for PAL and SECAM dual system color TV)

Parts	Specification
Coil For D.L. CCT	<p>① ~ ② 16 Turns ② ~ ③ 16 Turns ④ ~ ⑤ 16 Turns ⑤ ~ ⑥ 16 Turns</p> <p>Bobbin 10K type Pot Core: CT-31 Screw Core: C-2 Wire: 0.09φ 2UEW no load Q: 40</p>
Burst Cleaning and CW Phase Shift	<p>① ~ ③ 18 Turns</p> <p>Capacitor: 82PF RH type</p> <p>Bobbin: 10K type Pot Core: CT-31 Screw Core: C-2 Wire: 0.09φ 2UEW no load Q: 56</p>
D.L.	Type No. ADL-CS11 mfd by ASAHI GLASS CORP. JAPAN
X'tal	Type no. A9M2 mfd by Kinsekisha, Japan Load C: 16pF

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Parts	Specification
Bell Filter	 <p>① ~ ③ 32 Turns ④ ~ ⑥ 8 Turns Capacitor : 82PF RH type</p> <p>Bobbin : 10K type Pot Core : CT-31 Screw Core : C-2 Wire : 0.1φ 2UEW no load Q : 36</p>
Ident Coil	 <p>① ~ ③ 10 Turns with 2 wires (parallel)</p> <p>Bobbin : 10K type Pot Core : CT-31 Screw Core : C-2 Wire : 0.1φ 2UEW no load Q : 59</p>
Demo Coil	 <p>① ~ ③ 18 Turns</p> <p>Capacitor : 82PF RH type</p> <p>Bobbin : 10K type Pot Core : CT-31 Screw Core : C-2 Wire : 0.1φ 2UEW no load Q : 55</p>
D.L.	The D.L. of M51395AP is applied commonly.

A pot core and a screw core are manufactured by Taiyo Yuden, Japan.

Adjustment of electrical characteristic for PAL/SECAM dual system circuit M51395AP/M51397AP.

Adjustment is achieved as following sequence.

1. Bell filter transformer "T₁" (M51397AP)
Apply SECAM color signal to the input.
Adjust bell filter transformer "T₁" to make the color signal envelope at test point "TP₂" into flat.
2. Ident discriminator coil "L₁" (M51397AP)
Adjust ident discriminator coil "L₁" to give maximum ident filter voltage value at test point "TP₁".
3. Discriminator (Demodulator) coil "T₃/T₄" (M51397AP)
Adjust discriminator coil "T₃/T₄" to make the voltage of no color signal equal to the clamp voltage (~7.2V) at pins 18 and 22.
4. 4.433619MHz free run frequency (M51395AP)
Apply PAL B/W signal (no burst) to input, and connect 0.01μF between pin 1 and GND.

Connect high input impedance frequency counter at pin 17.

Adjust the trimmer capacitor "C_t" to frequency 4.433619MHz.

5. Burst cleaning coil "L₁₀" (M51395AP)

Apply PAL color signal to input.

Adjust burst cleaning coil "L₁₀" to give minimum chroma output signal value at pin 24.

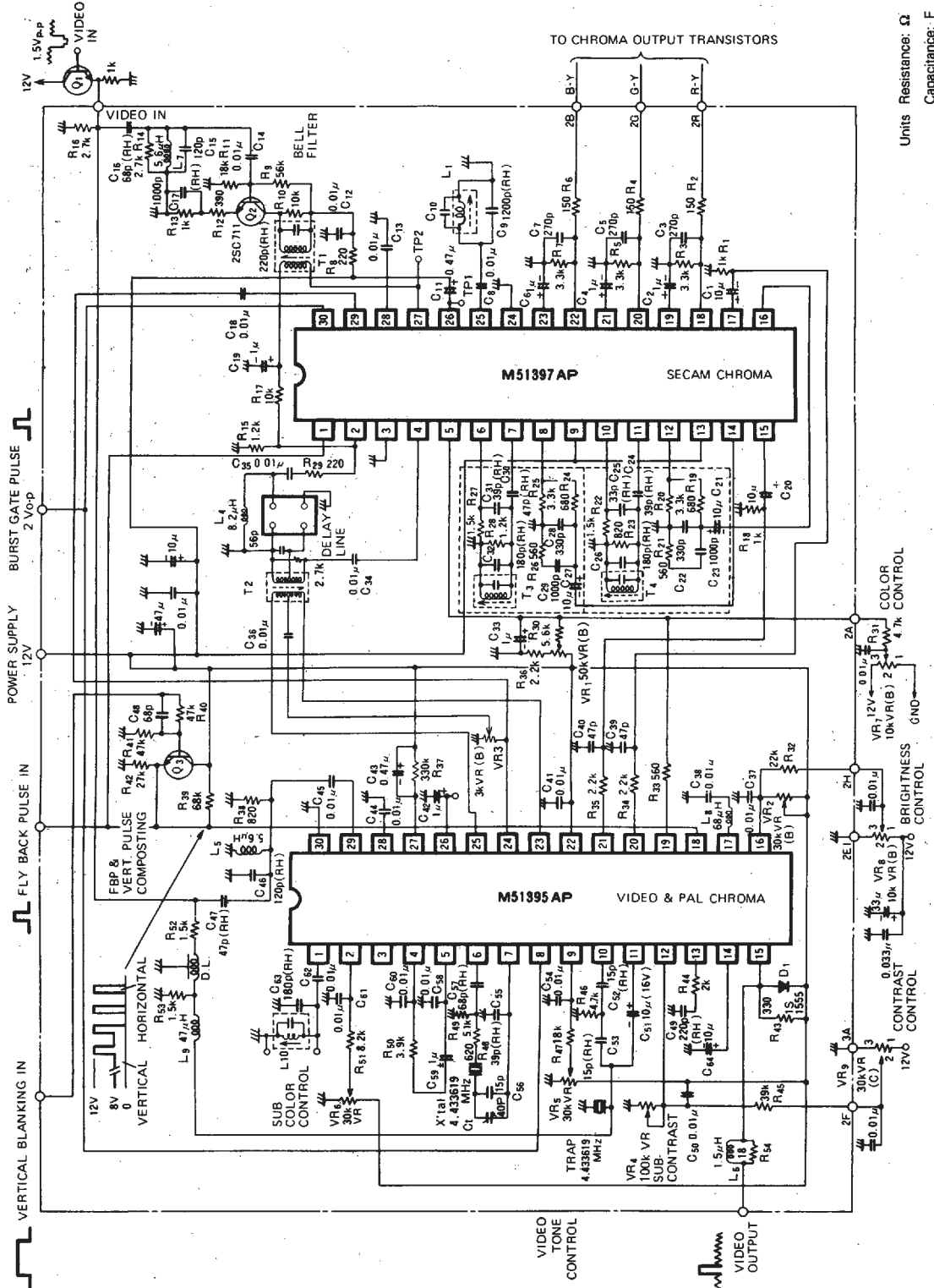
6. Delay line transformer "T₂", chroma difference signal control "VR₃" (M51395AP)

Adjust delay line transformer "T₂" and chroma difference signal control "VR₃" to correct demodulated ratios at pins 18, 20 and 22. If demodulated ratios are not correct, readjust burst cleaning coil "L₁₀".

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APPLICATION EXAMPLE



Units Resistance: Ω
Capacitance: F

M51397AP

SECAM CHROMA SYSTEM

M51395AP M51397AP PWB
PAL SECAM Dual System

Bottom View

