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ACP 2371 NI
Audio Processor
for Multistandard TV Sets

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Contents

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Audio Processor

Note:
If not otherwise designated, the pin numbers mentioned refer to the 44-pin PLCC package.

1. Introduction

The Audio Processor ACP2371NI comprises two components – an A/D converter (ADC) and an Audio Processor Unit (APU) implemented in CMOS (ADC) and NMOS (APU) technology.

Together with the MSP2410, the ACP2371NI is a true two-chip solution for terrestrial multistandard sound processing including NICAM and tone control for TV-Sets. One D/A converter pair represents the tone controlled output (DAC1) for speakers, the second D/A converter pair performs the conversion of digital sources (NICAM or FM from MSP) for the scart output (AUXOUT). Therefore DAC2 is routed to TVIN. Herewith it is possible to have an independent input selection for Speaker-Out and Scart-Out (e.g. NICAM to Speakers, FM to Scart).

The Audio Processor ACP2371NI has analog and digital inputs:

– Three analog stereo signal pairs are connected via analog switches with the analog output (AUXOUT) and the pulse-density modulators (PDM). Apart from the amplifiers at the inputs, there are also automatic level controls so that even overmodulated signals can be processed. The analog signals that are fed to the DSP unit are then passed to two pulse-density modulators which work on the sigma delta principle (PDM followed by conversion filters). The pulse train density at the PDM outputs is proportional to the signal amplitude; the PDM data rate is about 5 MHz. This high frequency means that anti-aliasing filters are not required. In the second step of the A/D conversion, in the digital decimation filters, the two PDM pulse trains are transformed into 16-bit words and the data rate to approx. 32 kHz, i.e. to values that are more favorable for subsequent processing. In terms of its signal-to-noise ratio, this combined converter system is more or less comparable to a conventional 16-bit A/D converter.

– The digital data bus, the S-Bus, was designed for the transmission of audio data from digital sources. Via the S-Bus Interface any digital source such as MSP 2410 IF-Processor or any DMA MAC-Decoder/Descrambler can be connected to the ACP2371NI. However, the ACP2371NI is prepared to work together with the MSP2410 as FM-Demodulator and NICAM-Decoder.

The activities of the various signal processors in the DIGIT 2000 System are coordinated via the Intermetall control bus (IM-Bus for short). A Central Control Unit (CCU) is used for this purpose. The CCU receives tuning instructions from the user and adjusts the corresponding registers of the signal processors to the required values. The CCU acts as a master, while the ACP and the other signal processors have purely slave status.

The DSP block consists of a mask-programmable digital signal processor with 256 x 14 bit ROM whose software can be controlled via the IM-Bus; in this way, various parameters (e.g. filter coefficients) can be altered during operation. The heart of the processor is a fast 16 x 8 multiplier, the basic instruction being the addition of products; this is performed in less than 250 ns. Other instructions (in particular, MOVE) can be executed simultaneously by the use of the pipelining technique so that the flow of arithmetic operations does not have to be interrupted. The clock frequency of the system of just 18 MHz means that a maximum of 5 million “product sums” can be calculated per second, which is adequate for real-time signal processing in the audio frequency range. All typical audio functions are carried out in the DSP block:

– Input selection between S-Bus and PDM data (NICAM from MSP, FM from MSP, Scart or AM via PDM)

– Dematrixing of the digital signals (necessary for two channel or stereo sound and mono modes)

– Adjustment of volume, balance, loudness, treble, bass, basewidth enlargement

– Independent input selection for Speaker-Out and Scart-Out (e.g. NICAM to Speakers, FM to Scart)

– Decoding of the identification signal of German 2-tone system for automatic switching between stereo, mono and bilingual sound modes. The three modes are identified by a characteristic frequency peak which is transmitted modulated upon a carrier of 54.6875 kHz (= three and a half times the horizontal frequency);

These tuning functions are controlled by the CCU via suitable filter coefficients and switches.

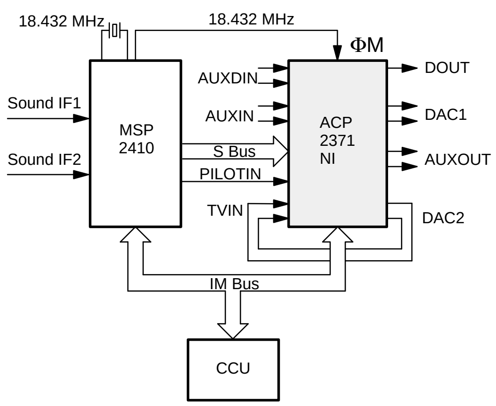


Fig. 1–1: Multistandard audio system with ACP237NI and MSP2410

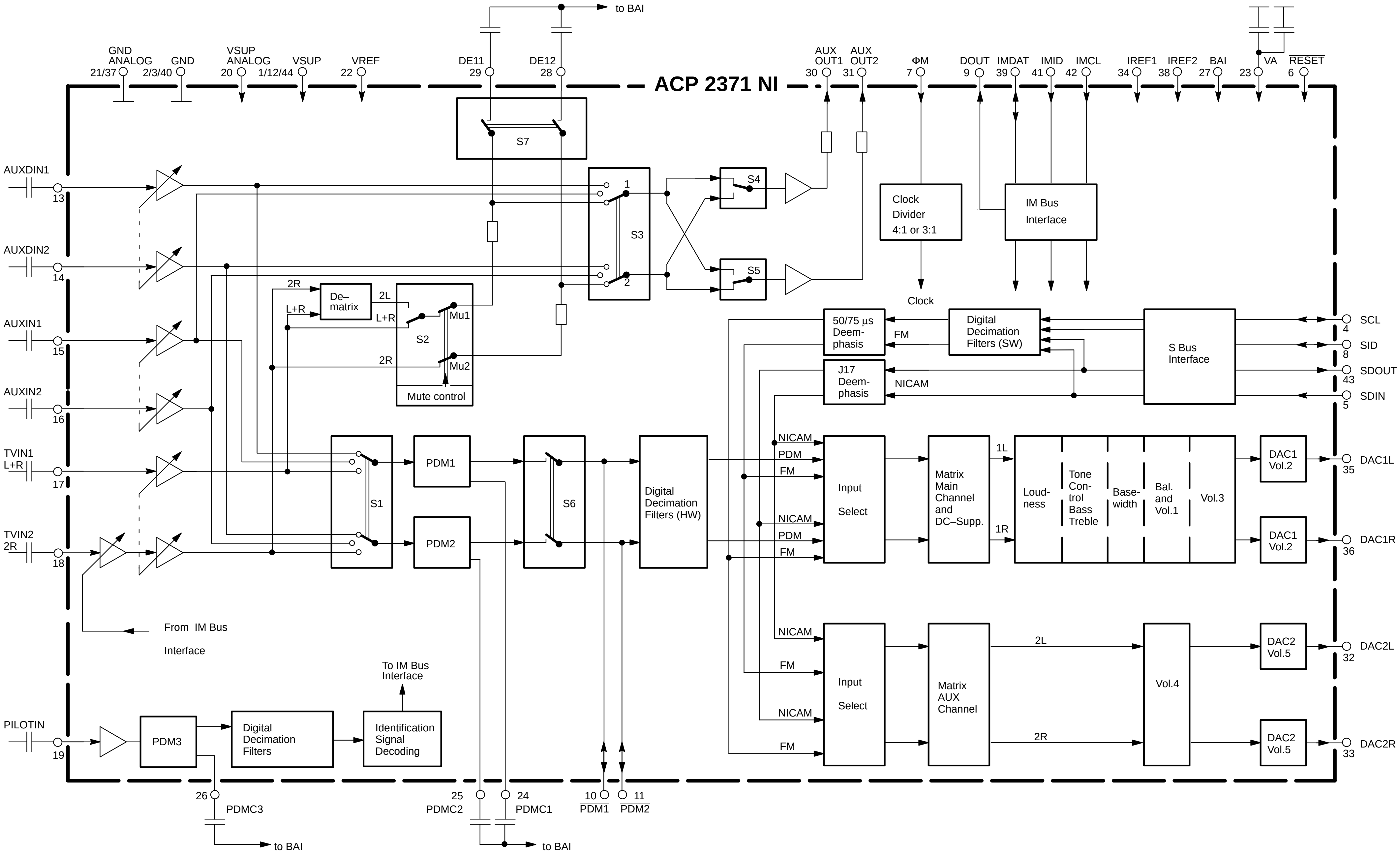


Fig. 1–2: Functional block diagram of the ACP 2371 NI

2. Functional Description of the A/D Part

The analog sound signals selected for conversion by the analog switches are fed to the first processing stage, the pulse density modulators PDM1 and PDM2. The output signals of these are 1-bit data streams at a rate of about 5 MHz. Due to the high sampling rate of the pulse density modulators no steep anti-aliasing filters are needed.

2.1. Analog Switches

The analog switches S1 to S7 are controlled via the IM bus (see section 2.6.).

S1 is used to select between signals from

– the FM-sound-demodulator of the TV set (inputs TVIN1, TVIN2)

– external sources, for example a video recorder (inputs AUXIN1, AUXIN2)

– additional audio sources, for example the output of the AM-sound-demodulator (inputs AUXDIN1, AUXDIN2)

S2 defines whether dematrixing is done or not, according to the German Zweiton TV stereo sound system (see Table 2–1). In addition, S2 is used to control a mute function for the SCART outputs (AUXOUT1, AUXOUT2).

S3 selects between signals from TVIN, AUXIN and an additional analog source fed to the inputs AUXDIN.

By means of switches S4 and S5, one single input signal can be connected to both AUXOUT outputs, e.g. if only one TVIN pin is supplied by a signal, as is the case whenever a non-stereo station is being received. In the case of a bilingual input, it is possible to cross the connections from language A and B to the outputs AUXOUT1 and AUXOUT2.

Controlled by the switch S6, the digital inputs/outputs 1 and 2 ($\overline{\text{PDM1}}$, $\overline{\text{PDM2}}$) either receive the pulse-density modulated output signals of another ADC or ACP, or serve as monitoring outputs of the pulse-density modulators PDM1 and PDM2. Their output signals can be fed, for example, to another ACP, APU or AMU.

2.2. Dematrix

When switched on via the IM bus (switch S2, (see Table 2–2), the dematrix provides the 2R and 2L stereo signals at the outputs AUXOUT. These signals are extracted from the L + R and 2R input signals (inputs TVIN) according to the German TV stereo sound system (see Table 2–1). If the MSP 2410 is used for FM-Demodulation, this is not necessary, because the dematrixing is done before D/A conversion in DAC2.

2.3. Pulse-Density Modulators

The two pulse-density modulators PDM1 and PDM2 are sigma-delta modulators equipped with two feedback loops each. At the outputs, they supply pulse trains whose pulse density is proportional to the amplitude of the input signal. The maximum sampling rate, and therefore, the maximum pulse rate is ΦM clock divided by 4.

2.4. Level Control

In former systems a certain signal level headroom had to be left free in order to avoid clipping and distortion in case of input levels beyond the nominal maximum. So some SNR was wasted. Using the internal level control in the ACP 2371NI, the input signal can be scaled up separately in each path. No external components are needed.

Whenever the input signal tends to exceed the PDM clipping level, a variable gain in the signal path is decreased in 16 steps, 1 step/ms until the modulation of the PDM is again well matched to the input level. If overload has disappeared the circuitry tries to increase the gain in 1 step/s until the internal signal level is at the optimum.

There is an additional gain adjustment for the input TVIN2 (±3 dB in steps of 0.2 dB) controlled by the IM bus, so that the channel separation can be optimized during production of the set (see Table 2–2). In the standard configuration (see Fig. 1–1), this feature is not used. Because matrixing is done digitally, no adjustments have to be made.

2.5. Preemphasis and Deemphasis or additional input for Scart-Out.

TV signals are always preemphasized with 50 µs according to the standard, AUXIN and AUXDIN signals normally are not. If the FM-Demodulation is not done in the MSP 2410, the deemphasis is realized as follows:

– apply deemphasis DE1 for AUXOUT path

– apply deemphasis at ACP outputs whenever S1 selects TVIN

Deemphasis DE1 is done by internal resistors and external capacitors.

DE11, DE12 could also be used as inputs for additional audio sources, selected by switch S7 and connected via S3 to AUXOUT. In this case, the Mute control Mu1, Mu2 has to be activated (Bit 3 of addr. 96), so that no other signal connected to AUXOUT. Then, the maximum input voltage is 260 mV RMS (with gain = 3.9 from DE1 to AUXOUT).

Table 2–1: Characteristics of the German TV stereo sound system

	FM1 (Mono)	FM 2
Carrier Frequency for sound	Sound Carrier: 5.5 MHz	Sound Carrier: 5.742 1875 MHz
Sound Signal Mono Stereo Bilingual	 Mono L + R Language A	 Mono 2 R Language B
Identification Signals Carrier Frequency Modulation Modulation Depth	 – – –	 $3.5 \cdot f_H = 54.6875$ kHz AM 50%
Identification Frequencies Mono Stereo Bilingual	 – – –	 unmodulated f_H: 133 ≈ 117.5 Hz f_H: 57 ≈ 274.1 Hz

2.6. Pilot Input

The pilot signal of the German Zweiton TV stereo sound system is transmitted on the second sound channel. This signal must be supplied separately to the input PILOTIN.

There is a separate A/D converter (PDM3 and digital decimation filter) for the input PILOTIN to avoid interaction between audio and pilot signals.

If the input PILOTIN is not used, it should be connected to ground.

2.7. IM Bus Interface

This circuit section is provided for controlling the A/D part by the CCU Central Control Unit.

In the case of the A/D part of the ACP 2371NI, the IM bus (see section 3.1.3.) is unidirectional from the CCU to the ACP. A one-bit data output (DOUT) for arbitrary use can be defined by the IM bus.

The bit arrangement is shown in Fig. 2–1 and the actions performed can be derived from Table 2–2.

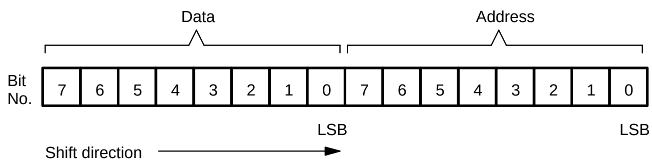


Fig. 2–1: Shape of the data word given from the CCU to the ACP

Table 2–2: Addresses and commands sent from the CCU to the A/D part of the ACP

Address Decimal	Bit No.	Function	Low Bit gives	High Bit gives
96	0	Switch S5	straight	cross
96	1	Switch S4	straight	cross
96	2	Switch S3	TVIN	AUXDIN
96	3	mute	feed through	mute
96	4	Switch S2	direct	dematrix
96	5	Switch S1	TVIN*	AUXIN*
96	6	DOUT	Low	High
96	7	Clock Divider	:4	:3
99	0	Additional	Bit 4 3 2 1 0	
99	1	gain adjustment	0 1 1 1 1 = max. gain = +3 dB	
99	2	of	0 0 0 0 0 = nom. gain = 0 dB	
99	3	input	1 0 0 0 0 = min. gain = – 3 dB	
99	4	TVIN2		
99	5	Switch S1	TVIN/AUXIN depending on Bit 5 of addr. 96	AUXDIN
99	6	Switch S6	PDM1, PDM2 = Outputs	PDM1, PDM2 = Inputs
99	7	Switch S7	Deemphasis ON	Deemphasis OFF
101	0	Switch S3	TVIN/AUXDIN depending on Bit 2 of addr. 96	AUXIN
101	1	Level Control AUXDIN1	as TVIN1	opposite to TVIN1
101	2	Level Control AUXDIN2	as TVIN2	opposite to TVIN2
101	3	Level Control AUXIN1	as TVIN1	opposite to TVIN1
101	4	Level Control AUXIN2	as TVIN2	opposite to TVIN2
101	5	Level Control TVIN1	Ch. 1 full gain	Ch. 1 sensed
101	6	Level Control TVIN2	Ch. 2 full gain	Ch. 2 sensed
101	7	Level Control	Level Control enabled	0 dB gain in all channels, Level Control disabled

* In the case that Bit 5 of address 99 is Low.

3. Architecture and Functional Description of the Audio Processor Part

The audio processor architecture combines two main parts: the I/O blocks and the DSP core. Fig. 3–1 shows a block diagram of the audio processor architecture.

3.1. I/O Blocks

3.1.1. Digital Decimation Filters

The digital decimation filters are cascades of transversal and recursive lowpass filters. They are necessary to convert the two 1-bit PDM-data streams by stepwise reduction of bandwidth and word rate (sampling rate) into two PCM data streams with 16 bit word length and a sampling rate of 32 kHz, which in the following are called PDM-Data 1 and 2. They are temporarily stored in the corresponding locations of the ACP Data RAM.

The two PDM-Data streams at the input of the decimation filters have no separate clock signal. Therefore, the decimation filters are equipped with a synchronization facility. This feature also supplies the ACP software with the sampling clock (32 kHz), which is called “I/O Sync”. More details about data/clock timing can be found in section 3.3.

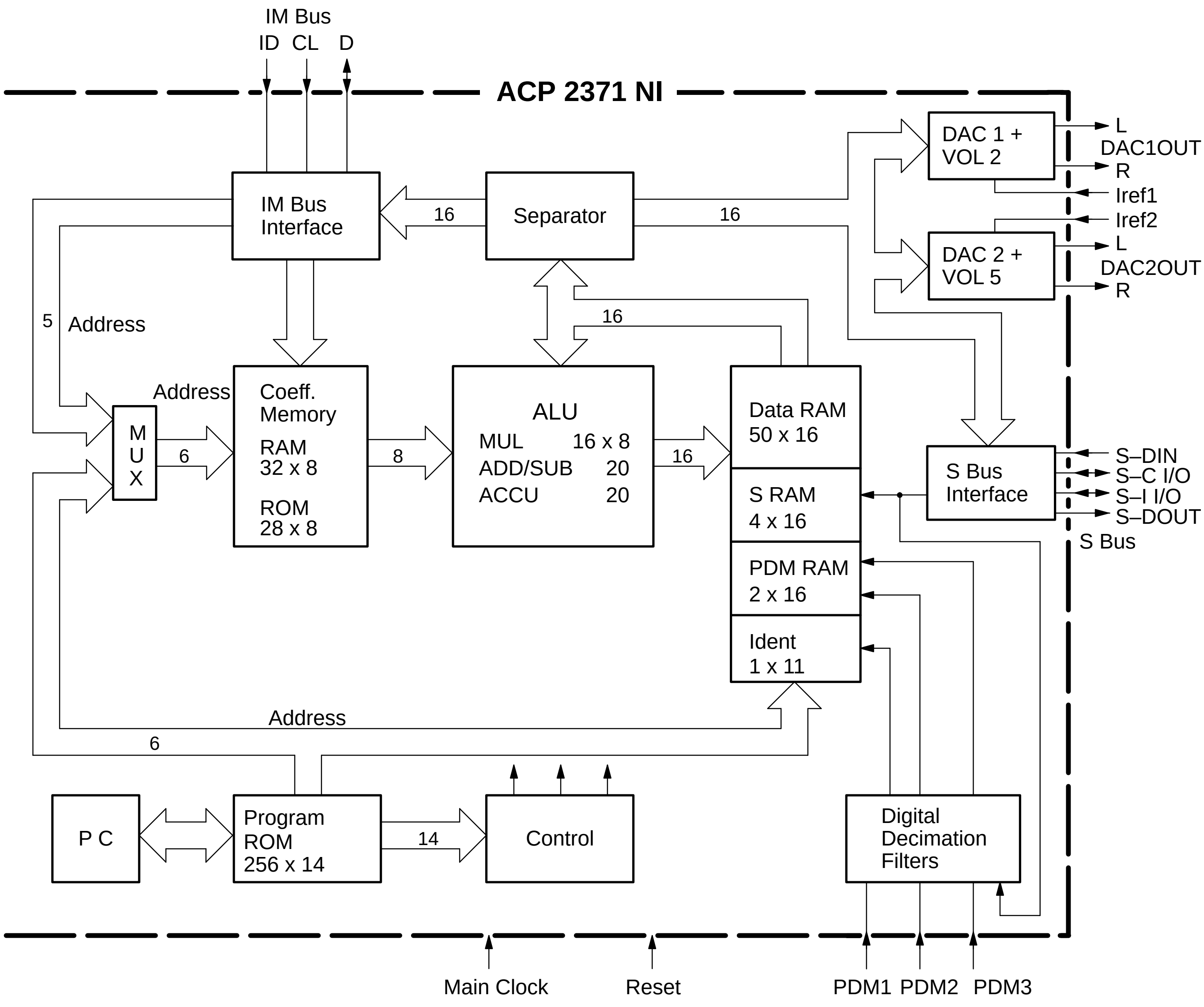


Fig. 3–1: ACP 2371 NI architecture of the audio processor part

3.1.2. S Bus Interface

Digital audio information provided by any digital source (for example DMA 2271, MSP 2410 or AMU 2481) is transmitted serially via the S bus to the S bus interface.

The S bus consists of four pins:

S-Data In: Four channels per sampling cycle (= 4 · 16 bits) are received from external circuits.

S-Data Out: Four channels per sampling cycle (= 4 · 16 bits) are transmitted to external circuits

S-Clock In/Out: gives the timing for the transmission of S-Data

S-Ident In/Out: after 64 S-Clock cycles the S-Ident determines the end of one sampling cycle

A precise timing diagram of the S bus is shown in Fig. 3–2. The S bus interface mainly consists of an input and output register, each having 64 bits. The timing to write or read out bit by bit is supplied by the S-Clock. In the case of an S-Ident pulse the contents of the input register are transferred to the Data RAM and the contents of the output register are written to the S-Data out line.

The S-Ident is also used as the sampling rate reference for the DSP software in the case of digital source mode. In this mode, the I/O-Sync, generated by the decimation filters is locked to the S-Ident. This allows a mixed mode, i.e. S-Data and PDM-Data can be processed simultaneously. However, this feature is not supported by the actual ACP 2371 NI software.

By means of coefficient k33 (see section 4.12.), the ACP 2371 NI can be switched to an S bus slave mode (bit 4=0) or to an S bus master mode (bit 4=1). The slave mode is required in an application as shown in Fig. 2–1, where the MSP 2410 NICAM Demodulator/Decoder acts as master on the S bus, i.e. the MSP supplies the S-Clock and S-Ident signals, as well as the S-Data input signal. In an application where two or more Audio Processors of the APU/ACP family are intended to work in one system without a DMA or MSP being present, one of the audio processors must act as master on the S bus (Table 4–22, notes).

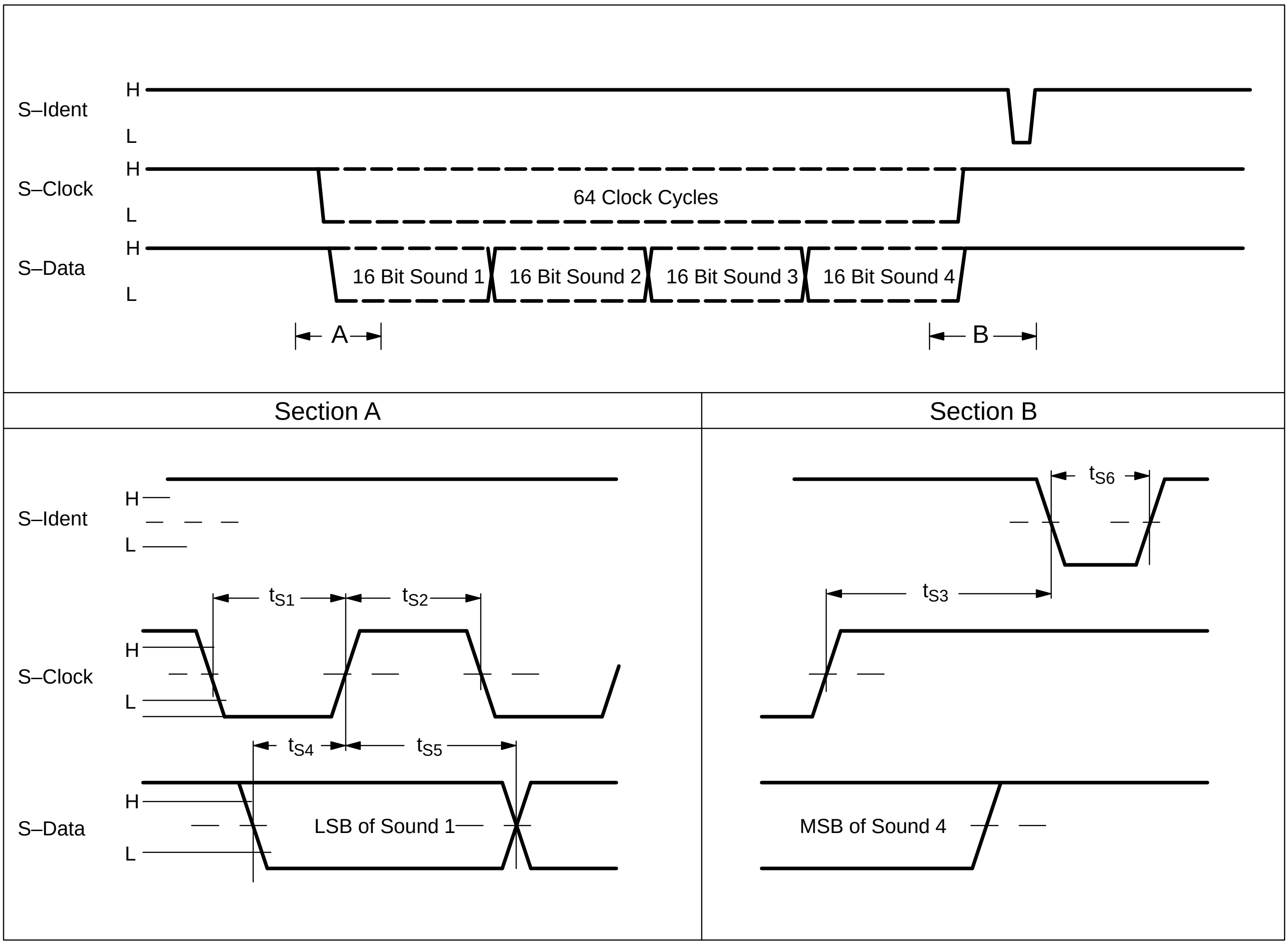


Fig. 3–2: S bus waveforms

3.1.3. IM Bus Interface and IM Bus

3.1.3.1. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM bus consists of three lines for the signals Ident (ID), Clock (CL), and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with on-resistances of 150 Ohm maximum. The 2.5 kOhm pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM bus transaction is shown in Fig. 3–3 and under “Recommended Operating Conditions”. In the non-operative state the signals of all three bus lines are High. To start a transaction, the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level as well to switch the first bit on the Data line. Thereafter, eight address bits are transmitted, beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave, the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address, the CCU now transmits eight or sixteen clock pulses, and accordingly, one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB. The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

For future software compatibility, the CCU must write a zero into all bits not used at present. When reading undefined or unused bits, the CCU must adopt “don’t care” behavior.

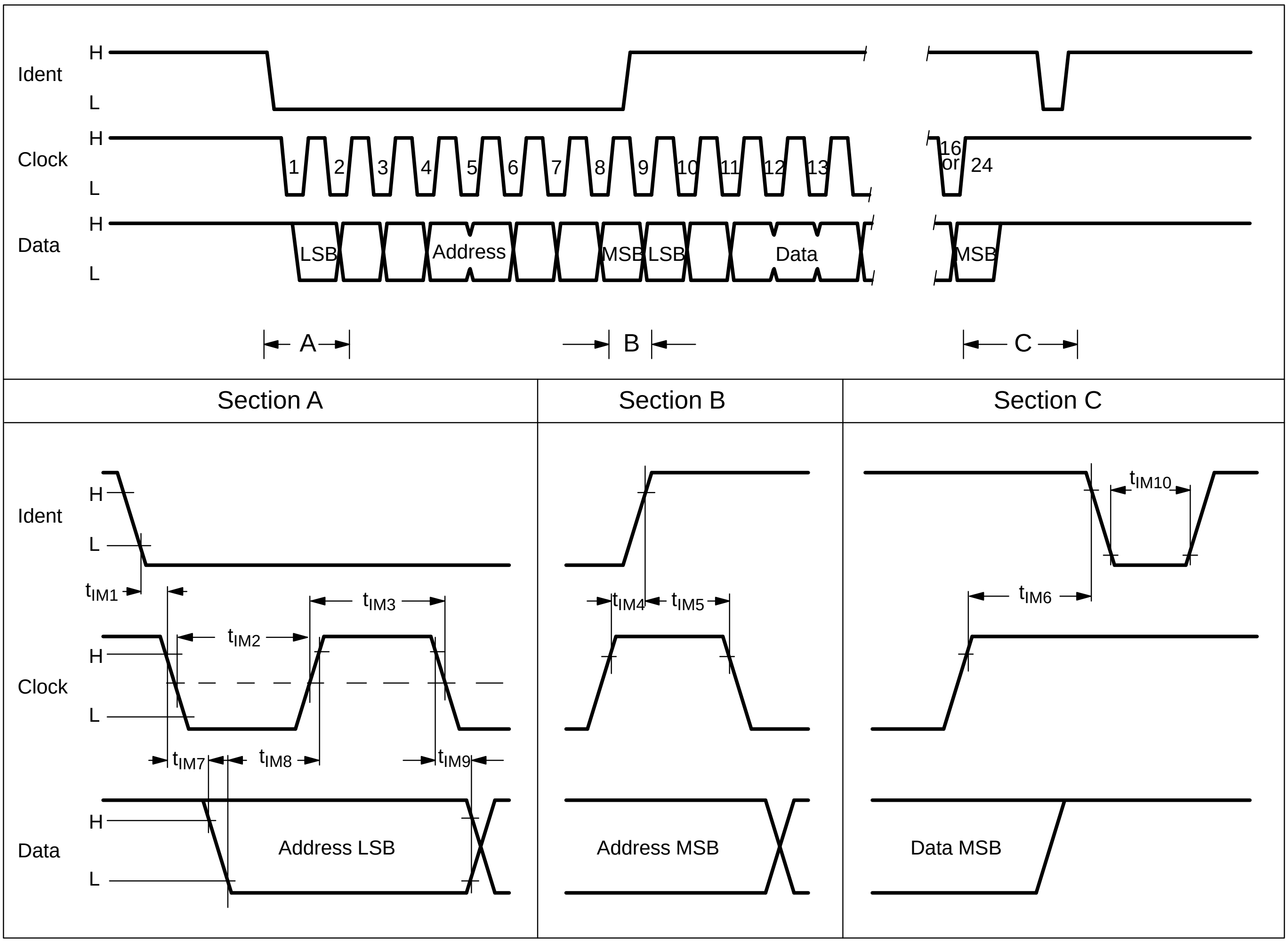


Fig. 3–3: IM bus waveforms

3.1.3.2. IM Bus Interface

Writing or reading coefficient value(s) into or from the ACP 2371 NI registers is done in the following steps:

1. addressing the ACP 2371 NI by the Select Register (allows multiprocessor system)
2. writing or reading of 8-bit data into or from IM bus interface registers.

When the ACP 2371 NI is addressed (step 1 above), the address transmitted first is 102 (= Select Register). If the following 8-bit data is identical to 00, further IM bus data will be accepted.

This kind of selective addressing allows controlling of different APU types (AMU 2481, ACP 2371) in a multi-APU system without using different address ranges. Each APU type will have its own (mask-programmed) select word. Note that in single ACP 2371 NI systems this select procedure can be omitted. The default select word is 00.

After having done step 1, step 2 can be performed as often as communication between ACP 2371 NI and the CCU is necessary, on condition that the processor address has not been changed by the CCU.

Comments to the steps mentioned above: The syntax of step 1 is identical to that of step 2. The CCU transmits an 8-bit address to the IM bus interface, addressing a certain register or C-RAM location of the ACP 2371NI. The IM bus interface has to check this address, and, if necessary, to store it and the following 8 data bits into special IM bus interface registers. Transfer of the data bits to the corresponding C-RAM locations is then performed by the ACP hardware at the sampling rate.

There is one value (IDLEV; see section 4.10.) which is read from the ACP to the CCU. This value is stored in the ACP's output buffer, address 63. If the CCU transmits this address, the IM bus interface writes the contents of the output buffer to the IM bus.

Addresses and data are transmitted with the LSB first. Transmission of one byte (8 bit) takes 100 µs. A spacing of 30 µs must be provided between the end of one transmission and the start of the next one.

3.1.4. Digital/Analog Converter (DAC) and Analog Volume

Digital to analog conversion is performed by four special conversion circuits. At any time, the current level of the output signals depends on the value of the reference currents, which are fed to pin 34 (for channel 1 converters DAC1) and to pin 38 (for channel 2 converters DAC2). Fig. 3–4 gives application diagrams for the DAC circuits. The network to be seen after the DACs perform a 5 µs analog lowpass.

Note:
There is an application restriction with the above converters: The clock rate of the ACP must fulfil the following clock condition:

Clock rate = sampling rate · n · 16

with n being an integer value. In section 3.3. all clocks relevant for ACP application are listed. They fulfil the above condition.

To improve the signal-to-noise ratio of the ACP 2371 NI (especially for low volume settings) an additional volume control facility is provided after the DACs. Digitally adjusted attenuators act in 29 steps of 1 dB each. More about Volume 2 and 5 in section 4.6.

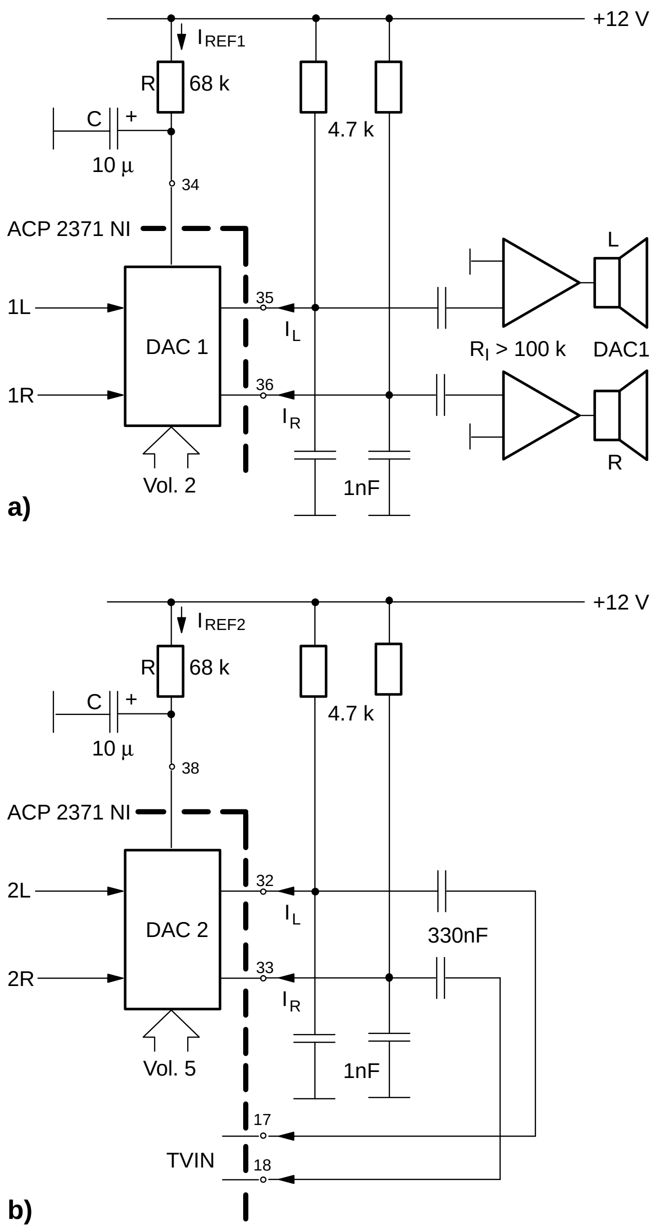


Fig. 3–4: DAC application diagrams
a) DAC 1 Interface (Speakers)
b) DAC 2 Interface (wired to TVIN)

3.2. DSP Block

The ACP 2371 NI contains a complete mask-programmable digital signal processor with the blocks as described in the following sections.

3.2.1. C-RAM, C-ROM and Data RAM

Coefficients and control parameters for digital processing of audio data are either fixed or variable by means of the CCU. The coefficient (C) memory is therefore divided into two parts:

1. C-RAM, containing 32 8-bit locations, which can be loaded by the CCU via the IM bus interface. The software needs 32 variable parameters, and for proper processing, all locations must be loaded with the corresponding values.
2. C-ROM, containing 28 8-bit locations, which are loaded with fixed values, needed for the DSP software. For the user, there is no possibility to change coefficients in the C-ROM.

Input data and intermediate results can be stored in the Data RAM of the ACP 2371 NI. It is arranged in the following way:

– 50 locations for intermediate results and output data

– 4 locations for S bus input channels

– 2 locations for 2 PDM channels from the decimation filters

– 1 location for identification signal

All locations have 16 bit word length.

3.2.2. Program ROM, Program Counter and Control

The DSP software of the ACP 2371 NI is stored in the program ROM. Its size is 256 · 14 bits and its content cannot be modified by the user (mask-programmed). Program ROM is addressed by the program counter (P.C.), which is a presettable counter.

Instruction decoding and coordinating of all time functions is performed by the control block. Multiplexing of the two busses, addressing the coefficient memory, and controlling the separator are also tasks of the control block. By means of the separator, data are transferred either to the IM bus output buffer (see section 4.10.) or to the DACs.

3.2.3. Arithmetic Logic Unit (ALU)

The core of the DSP block is the ALU. Multiplication of 16 · 8 bit, adding using a 20-bit accumulator, and shift operations are performed in the ALU. Accumulation is done according to a saturation characteristic (see section 4.1.).

3.3. System Clock ΦM and PDM Sampling Rate

The clock at the ACP's ΦM input must be 18.432 MHz, due to its software structure. Therefore, bit 2 of k33 has to be set to 1 all the time. The resulting PDM and sampling rates are:

– PDM rate	= ΦM : 4	= 4.608 MHz,
– sampling rate	= ΦPDM : 144	= 32 KHz

The physical source of the ACP's system clock is the MSP 2410, the DMA 2271, or the MCU.

Table 3-1: Selection of operation mode

Input	k33	Bit 7	Bit 6	Bit 2
SBUS connected to MSP		0	1	1
No SBUS connected		0	0	1

Note: Selection of the operation mode (clock dividers) is to be transmitted by the CCU by means of bit 7/6/2 of k33).

4. Functions Performed by DSP Software

4.1. Explanation of Typical DSP Symbols and Representation of Numbers

In the following, all software features are explained in terms of signal flow diagrams and coefficient tables. In the appendix there is also a complete program structure of the ACP 2371 NI software. In order to apply these instructions in a correct manner, some explanations are required:

Symbols of Signal Flow Diagrams

⊕	adder
⊗	multiplication with coefficient
SHAL	shift arithmetic left (multiplication by 2)
ki, Cj	coefficient: ACP internal address (Table 4–22) k = coefficients controlled by CCU and after transfer stored in the ACP's C-RAM, C = fixed coefficient in the ACP's C-ROM
48 15	z^{1} Term: delay by one sampling clock cycle, realized by one or (in case of two parallel channels) two memory locations of the C-RAM. The numbers are the ACP memory addresses.

Representation of Numbers

The ACP 2371 NI has a two's complement, fixed point arithmetic with decimal point being left-hand and the MSB being the sign bit. The word lengths are defined as follows:

- coefficients: 8 bits including sign bit
- data at multiplier input: 16 bits including sign bit
- intermediate results: 20 bits including sign bit

Table 4–2 shows as an example the range of the 8-bit coefficients, resulting from the conditions mentioned above. From the view of the CCU programmer, this might be the most interesting case. Three formats are used to express the coefficient values: integer decimal, integer hexadecimal, and normalized.

Coefficient values must be transferred from the CCU to the ACP via the IM bus in binary format; therefore in most tables of this data sheet, the values will be presented in HEX, and additionally, in the normalized format to make the digital signal processing background more understandable. To save space, the normalized values will be rounded.

Note: Coefficients kij have to be determined such that any overflow in the ACP arithmetic is excluded. Nevertheless, if overflow occurs, the ALU will deal with it according to a saturation characteristic. Considering this restriction, for good S/N ratio the digital range must be optimally used. This means, that for controlling bass or treble, a volume adjustment will in most cases be necessary (see sections 4.6. to 4.8.).

4.2. Digital Deemphasis

4.2.1. J17 for NICAM

While NICAM is always J17 preemphasized, an unswitchable J17 deemphasis is implemented in the NICAM signal path.

Note: The feature, J17 deemphasis, is not controllable by the CCU because all coefficients are fixed and stored in the ACP's C-ROM.

4.2.2. 50 µs/75 µs and SW-CF2 for FM

The digital sound data coming from the MSP in FM mode have a sampling frequency of 64 kHz. They are downsampled in conversion filter 2, implemented by the software. The deemphasis filter is combined with this filter block.

FM modulated signals are usually preemphasized with a RC-network having a time constant of 50 µs or 75 µs. Therefore, the ACP 2371NI provides a deemphasis filter that can be switched either to 50 µs, 75 µs or off.

Table 4–1: Coefficient for deemphasis and conversion filter (hex/norm)

Function	Coefficient	Value
50 µs	k18 k31	45; 0.539 FB; –0.039
75 µs	k18 k31	54; 0.656 FC; 0.031
OFF	k18 k31	00; 0.000 EA; –0.171

Table 4–2: Range of an 8-bit coefficient value

Coefficient	ACP Internal Presentation	HEX	DEC	Normalized
Max. Value Min. Positive Number	0111 1111 0000 0001	7F 01	127 001	0.9921875 0.0078125
Max. Negative Number Min. Number	1111 1111 1000 0000	FF 80	255 128	–0.0078125 –1.0

4.3. Input Select

The ACP 2371 NI is provided to process audio data coming from three sources, whereby the controllable input select software switches to the one chosen by the CCU:

1. PDM-Data coming from the A/D converter via digital decimation filters (HW-CF).

– TVIN, AUXIN or AUXDIN ⇒ PDM1/2

2. FM-Data coming from the SBUS Interface via conversion filter 2 implemented in software (SW-CF2).

– S_CH1 & S_CH2 ⇒ FM1

– S_CH3 & S_CH4 ⇒ FM2

3. NICAM-Data coming from the SBUS Interface

– S_CH3 ⇒ NICAM A or NICAM L

– S_CH4 ⇒ NICAM B or NICAM R

4.3.1. Channel1 (Speaker-Out)

All three sources can be routed to DAC1 Out by means of coefficients K23, K24, K25.

Table 4–3: K23/K24/K25 depending on input source

Input Source	k23	k24	k25
PDM-Data FM-Data NICAM-Data	7F 00 00	00 7F 00	00 00 7F

4.3.2. Channel 2 (Output wired to TVIN)

Channel 2 is working as a D/A Converter for NICAM or FM to Scart-Out. Therefore, it is not necessary to be able to route PDM1/2 to DAC2. Input select is done by means of coefficient K13.

Table 4–4: K13 due to input source

Input Source	k13
FM-Data NICAM-Data	80 7F

4.4. Dematrixing

To achieve compatibility with standard mono TV sets and to realize bilingual audio performance, the German TV stereo system was defined according to Table 4–7. Additionally, the sound format of SCART sources is listed. In TV receivers, these characteristics require dematrixing of the two channels.

After detection and evaluation of the identification signal, (see section 4.10.) the NICAM status bits, and the remote control status, the CCU transmits two coefficient sets according to the current operation mode. The ACP dematrixing, processed both in channel 1 and 2, provides the following audio possibilities for each channel separately (Fig. 4–1):

– mono

– stereo

– bilingual 0: language A on left
language B on right

– bilingual 1: language B on left
language A on right

– bilingual 2: language A on left & right

– bilingual 3: language B on left & right

In the following Tables 4–5 and 4–6, all relevant coefficients and the corresponding operation modes (see above) are listed. Because of the different processing for different sources, a volume prescale has to be done. For that reason, the matrix coefficients vary for each source. Table 4–8 gives the corresponding values.

To avoid switching distortions in the case of operation mode change, it is recommended to alter the coefficients in steps of 10 units maximum rather than instantaneously.

Table 4–5: Coefficients for channel 1 dematrixing

Coeff.	Mono	Stereo Modes			Bilingual Modes			
		FM	NICAM	SCART	0	1	2	3
k14	SCALE	2*SCALE	SCALE	SCALE	SCALE	00	SCALE	00
k15	00	SCALE	SCALE	SCALE	SCALE	00	00	SCALE
k16	00	– SCALE	00	00	00	SCALE	00	SCALE
k17	SCALE	00	00	00	00	SCALE	SCALE	00

Table 4–6: Coefficients for channel 2 dematrixing

Coeff.	Mono	Stereo Modes			Bilingual Modes			
		FM	NICAM	SCART	0	1	2	3
k19	SCALE	2*SCALE	SCALE	SCALE	SCALE	00	SCALE	00
k20	00	SCALE	SCALE	SCALE	SCALE	00	00	SCALE
k21	00	– SCALE	00	00	00	SCALE	00	SCALE
k22	SCALE	00	00	00	00	SCALE	SCALE	00

Table 4–7: Characteristics of German FM Stereo system

	FM1 (Mono)	FM2
1. Sound Signal from TV Channel		
Mono Stereo Bilingual	Mono (L = R) L + R Language A	– 2 R Language B
2. Sound signal from SCART Input		
Mono Stereo Bilingual	Mono (L = R) L Language A	Mono (L = R) R Language B

a)

b)

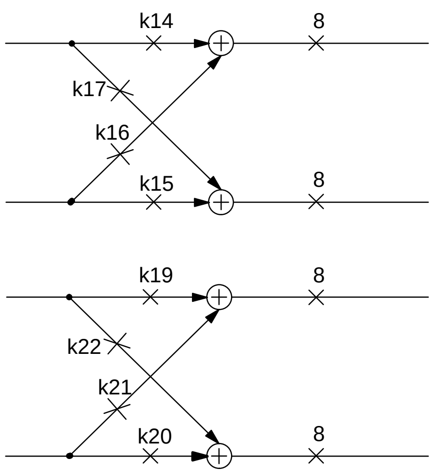


Fig. 4–1: Matrix filter structure
a) Channel 1 b) Channel 2

Table 4–8: Normalized values of variable “SCALE” in Tables 4–5 and 4–6

Input Selected	HEX	DEC	Normalized
PDM	20	32	0.25
FM 50 kHz 75 kHz 150 kHz	2A 1C 0E	42 28 14	0.328125 0.492188 0.109375
NICAM	34	52	0.406250

4.5. DC Offset Suppression (only for Channel 1)

To avoid audible distortions caused by volume changes, the DC part of the signals coming from the decimation filters has to be minimized. Therefore, DC suppression for channel 1 is performed.

Note: The feature, DC offset suppression, is not controllable by the CCU because all coefficients are fixed and stored in the ACP’s C-ROM.

4.6. Balance and Volume Setting

4.6.1. Channel 1

To maintain a high signal-to-noise ratio even with low input levels or at low volume, the complete volume adjustment is performed in three single stages:

1. VOL 1 (digital): Is determined by the coefficients k0 (right channel) and k1 (left channel). By means of separate coefficients for each channel, the CCU can additionally provide balance information.
Range: k0/1 = 0 to 0.9921875 = 0 to 7Fhex

2. VOL 2: Analog volume adjustment after the DACs. The audio analog outputs left and right are controlled by a digitally adjusted attenuator, which is derived from k34 in steps of one dB, the total number of steps being 29.
Range: k34 = 0 to 0.2265625 = 0 to 1Dhex
(–29 dB to 0 dB)

By means of the two volume adjustments mentioned above, an overall level of 0 dB is attainable. In the case of small input signals, a third volume adjustment is provided (see recommendations of sections 4.7. and 4.8.).

3. VOL 3 (digital): Using k2, a gain of further 12 dB is possible. The complete volume 3 adjustment is realized by multiplication by k2 and a shift left of 2 bits (· 4).
Range: k2 = 0.25 to 0.99 = 20hex to 7Fhex

Recommendations:
The overall volume range is listed in Table 4–9. To avoid overmodulations, only the range up to +6 dB is used. The values, which change from low to high volume, are printed in bold type.

The range up to +6 dB, provided by volume 3, should be saved only for volume adjustments necessary in the case of certain bass or treble requirements (see section 4.9.). This means, that with linear bass and treble status only 0 dB is achievable by means of the remote control unit.

Increasing and decreasing of volume must be done in steps of 1 dB; adjust, if table calculation makes necessary, with the following sequence:

1. VOL 1
2. k5 (Loudness)
3. VOL 2
4. VOL 3

Muting on (current volume to volume = 0):
The muting on or off functions must be solved in such a way that the number of transferred coefficients is always constant (87), i.e., independent of the current volume value. This means that for a certain current volume value not only the m coefficients to decrease volume have to be transferred, but also n times the coefficient of the current value. With n+m = 87 the condition above is fulfilled. The sequence to change, if necessary, the volume coefficients is the following:

1. VOL 3 if necessary
2. k5 and VOL 2 (toggling) if necessary
3. VOL 1 (k0 and k1 toggling) if necessary

Muting off (volume = 0 to current volume):
The same procedure as for muting on, but in reverse direction. The number of transferred coefficients per muting off function must also be constant (87).

4.6.2. Channel 2

The channel 2 volume control is performed in one stage:

1. VOL 5 (analog): This is an analog attenuation after the DACs (see VOL 2). It is controlled by k39 (Bit 0 to Bit 4) in 1 dB steps.

Range: k39 = 0 to 0.2265625 = 0 to 1Dhex
(–29 dB to 0 dB)

VOL 5 is set to maximum during RESET. Table 4–10 shows the volume control for channel 2.

4.7. Loudness (only for Channel 1)

To compensate for the characteristics of human hearing, which is less sensitive to bass and treble at low volumes than at high volumes, the ACP provides a loudness function. All coefficients necessary for this filtering, with the exception of one (k5) are fixed and stored in the ACP's CROM. Modifying k5 by the CCU allows a volume-dependent loudness function. An example of volume-dependent loudness is shown in Table 4–9. Fig. 4–2 presents the corresponding frequency response. It is obvious that for
k5 = 0 loudness is most effective (for low volume),
and for
k5 = 127 = 7hex loudness is off (for high volume).

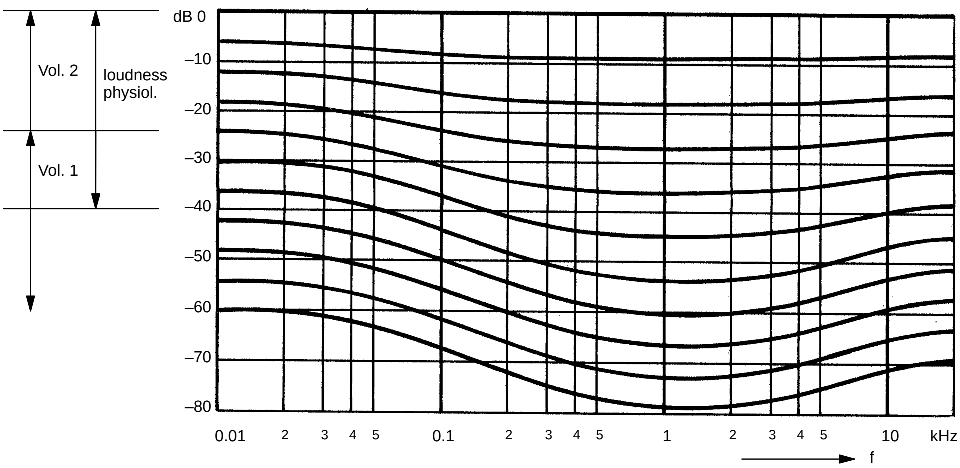


Fig. 4–2: Frequency response of Loudness combined with volume (example)

Table 4–9: Volume and loudness coefficients (HEX and normalized) with bass and treble responses being linear

Volume Value	Overall Level/dB	VOL 1 k0/1	VOL 2 k34	VOL 3 k2	Loudness k5
87	6	7F; 0.99	1D; 0.23	**40; 0.5**	7F; 0.99
86	5	7F; 0.99	1D; 0.23	**39; 0.45**	7F; 0.99
85	4	7F; 0.99	1D; 0.23	**33; 0.4**	7F; 0.99
84	3	7F; 0.99	1D; 0.23	**2D; 0.35**	7F; 0.99
83	2	7F; 0.99	1D; 0.23	**28; 0.31**	7F; 0.99
82	1	7F; 0.99	1D; 0.23	**24; 0.28**	7F; 0.99
81	0	7F; 0.99	**1D; 0.23**	20; 0.25	7F; 0.99
80	– 1	7F; 0.99	**1C; 0.22**	20; 0.25	7F; 0.99
79	– 2	7F; 0.99	**1B; 0.21**	20; 0.25	7F; 0.99
78	– 3	7F; 0.99	**1A; 0.20**	20; 0.25	7F; 0.99
77	– 4	7F; 0.99	**19; 0.19**	20; 0.25	7F; 0.99
76	– 5	7F; 0.99	**18; 0.18**	20; 0.25	7F; 0.99
75	– 6	7F; 0.99	**17; 0.18**	20; 0.25	7F; 0.99
74	– 7	7F; 0.99	**16; 0.17**	20; 0.25	7F; 0.99
73	– 8	7F; 0.99	**15; 0.16**	20; 0.25	7F; 0.99
72	– 9	7F; 0.99	14; 0.15	20; 0.25	**7F; 0.99**
71	–10	7F; 0.99	**14; 0.15**	20; 0.25	72; 0.89
70	–11	7F; 0.99	13; 0.15	20; 0.25	**72; 0.89**
69	–12	7F; 0.99	**13; 0.15**	20; 0.25	66; 0.8
68	–13	7F; 0.99	12; 0.14	20; 0.25	**66; 0.8**
67	–14	7F; 0.99	**12; 0.14**	20; 0.25	5B; 0.71
66	–15	7F; 0.99	11; 0.13	20; 0.25	**5B; 0.71**
65	–16	7F; 0.99	**11; 0.13**	20; 0.25	51; 0.63
64	–17	7F; 0.99	10; 0.12	20; 0.25	**51; 0.63**
63	–18	7F; 0.99	**10; 0.12**	20; 0.25	48; 0.56
62	–19	7F; 0.99	0F; 0.11	20; 0.25	**48; 0.56**
61	–20	7F; 0.99	**0F; 0.11**	20; 0.25	40; 0.5
60	–21	7F; 0.99	0E; 0.11	20; 0.25	**40 0.5**
59	–22	7F; 0.99	**0E; 0.11**	20; 0.25	39; 0.45
58	–23	7F; 0.99	0D; 0.10	20; 0.25	**39; 0.45**
57	–24	7F; 0.99	**0D; 0.10**	20; 0.25	33; 0.4
56	–25	7F; 0.99	0C; 0.09	20; 0.25	**33; 0.4**
55	–26	7F; 0.99	**0C; 0.09**	20; 0.25	2D; 0.35
54	–27	7F; 0.99	0B; 0.08	20; 0.25	**2D; 0.35**
53	–28	7F; 0.99	**0B; 0.08**	20; 0.25	28; 0.31
52	–29	7F; 0.99	0A; 0.08	20; 0.25	**28; 0.31**
51	–30	7F; 0.99	**0A; 0.08**	20; 0.25	24; 0.28
50	–31	7F; 0.99	09; 0.07	20; 0.25	**24; 0.28**
49	–32	7F; 0.99	**09; 0.07**	20; 0.25	20; 0.25
48	–33	7F; 0.99	08; 0.06	20; 0.25	**20; 0.25**
47	–34	7F; 0.99	**08; 0.06**	20; 0.25	1D; 0.23
46	–35	7F; 0.99	07; 0.05	20; 0.25	**1D; 0.23**
45	–36	7F; 0.99	**07; 0.05**	20; 0.25	1A; 0.20
44	–37	7F; 0.99	06; 0.05	20; 0.25	**1A; 0.20**
43	–38	7F; 0.99	**06; 0.05**	20; 0.25	17; 0.18
42	–39	7F; 0.99	05; 0.04	20; 0.25	**17; 0.18**
41	–40	7F; 0.99	**05; 0.04**	20; 0.25	14; 0.16
40	–41	7F; 0.99	04; 0.03	20; 0.25	**14; 0.16**

Table 4–9, continued

Volume Value	Overall Level/dB	VOL 1 k0/1	VOL 2 k34	VOL 3 k2	Loudness k5
39	–42	7F; 0.99	**04; 0.03**	20; 0.25	12; 0.14
38	–43	7F; 0.99	03; 0.02	20; 0.25	**12; 0.14**
37	–44	7F; 0.99	**03; 0.02**	20; 0.25	10; 0.12
36	–45	7F; 0.99	02; 0.02	20; 0.25	**10; 0.12**
35	–46	7F; 0.99	**02; 0.02**	20; 0.25	0E; 0.11
34	–47	7F; 0.99	01; 0.01	20; 0.25	**0E; 0.11**
33	–48	7F; 0.99	**01; 0.01**	20; 0.25	0D; 0.10
32	–49	**7F; 0.99**	00; 0.0	20; 0.25	0D; 0.10
31	–50	**71; 0.88**	00; 0.0	20; 0.25	0D; 0.10
30	–51	**65; 0.79**	00; 0.0	20; 0.25	0D; 0.10
29	–52	**5A; 0.70**	00; 0.0	20; 0.25	0D; 0.10
28	–53	**51; 0.63**	00; 0.0	20; 0.25	0D; 0.10
27	–54	**48; 0.56**	00; 0.0	20; 0.25	0D; 0.10
26	–55	**40; 0.5**	00; 0.0	20; 0.25	0D; 0.10
25	–56	**39; 0.45**	00; 0.0	20; 0.25	0D; 0.10
24	–57	**33; 0.4**	00; 0.0	20; 0.25	0D; 0.10
23	–58	**2D; 0.35**	00; 0.0	20; 0.25	0D; 0.10
22	–59	**28; 0.31**	00; 0.0	20; 0.25	0D; 0.10
21	–60	**24; 0.28**	00; 0.0	20; 0.25	0D; 0.10
20	–61	**20; 0.25**	00; 0.0	20; 0.25	0D; 0.10
19	–62	**1D; 0.23**	00; 0.0	20; 0.25	0D; 0.10
18	–63	**1A; 0.20**	00; 0.0	20; 0.25	0D; 0.10
17	–64	**17; 0.18**	00; 0.0	20; 0.25	0D; 0.10
16	–65	**14; 0.16**	00; 0.0	20; 0.25	0D; 0.10
15	–66	**12; 0.14**	00; 0.0	20; 0.25	0D; 0.10
14	–67	**10; 0.12**	00; 0.0	20; 0.25	0D; 0.10
13	–68	**0E; 0.11**	00; 0.0	20; 0.25	0D; 0.10
12	–69	**0D; 0.10**	00; 0.0	20; 0.25	0D; 0.10
11	–70	**0B; 0.09**	00; 0.0	20; 0.25	0D; 0.10
10	–71	**0A; 0.08**	00; 0.0	20; 0.25	0D; 0.10
9	–72	**09; 0.07**	00; 0.0	20; 0.25	0D; 0.10
8	–73	**08; 0.06**	00; 0.0	20; 0.25	0D; 0.10
7	–74	**07; 0.05**	00; 0.0	20; 0.25	0D; 0.10
6	–76	**06; 0.05**	00; 0.0	20; 0.25	0D; 0.10
5	–77	**05; 0.04**	00; 0.0	20; 0.25	0D; 0.10
4	–79	**04; 0.03**	00; 0.0	20; 0.25	0D; 0.10
3	–82	**03; 0.02**	00; 0.0	20; 0.25	0D; 0.10
2	–85	**02; 0.02**	00; 0.0	20; 0.25	0D; 0.10
1	–91	**01; 0.01**	00; 0.0	20; 0.25	0D; 0.10
0	mute	00; 0.00	00; 0.0	20; 0.25	0D; 0.10

Table 4–10: Volume control for channel 2

Overall Level/dB	VOL 4 k6		VOL 5 k39	
0	5C;	0.71875	1D;	0.227
–1	5C;	0.71875	1C;	0.219
–2	5C;	0.71875	1B;	0.211
–3	5C;	0.71875	1A;	0.203
–4	5C;	0.71875	19;	0.195
–5	5C;	0.71875	18;	0.188
–6	5C;	0.71875	17;	0.180
–7	5C;	0.71875	16;	0.172
–8	5C;	0.71875	15;	0.164
–9	5C;	0.71875	14;	0.156
–10	5C;	0.71875	13;	0.148
–11	5C;	0.71875	12;	0.141
–12	5C;	0.71875	11;	0.133
–13	5C;	0.71875	10;	0.125
–14	5C;	0.71875	0F;	0.117
–15	5C;	0.71875	0E;	0.109
–16	5C;	0.71875	0D;	0.102
–17	5C;	0.71875	0C;	0.094
–18	5C;	0.71875	0B;	0.086
–19	5C;	0.71875	0A;	0.078
–20	5C;	0.71875	09;	0.070
–21	5C;	0.71875	08;	0.063
–22	5C;	0.71875	07;	0.055
–23	5C;	0.71875	06;	0.047
–24	5C;	0.71875	05;	0.039
–25	5C;	0.71875	04;	0.031
–26	5C;	0.71875	03;	0.023
–27	5C;	0.71875	02;	0.016
–28	5C;	0.71875	01;	0.008
–29	5C;	0.71875	00;	0.000

4.8. Bass and Treble Control and its Effects on Volume (only for Channel 1)

In the channel 1, adjustment of treble and bass is done by separate first order recursive filters. A block diagram is shown in Fig. 4–3.

Treble adjustment is done by the coefficients k7, k8 and k9. to avoid any data overflow caused by treble boosting, it is recommended not to lift high frequencies, but to reduce low frequencies and to increase the overall volume level. Table 4–11 gives an application example for k7, k8 an k9: Treble control range –12 dB to +12 dB in 1 dB steps. Fig. 4–4 shows the treble frequency response of every third step.

Bass adjustment is done by the coefficients k10, k11 and k12. Data overflow has to be avoided here also. Partly, this is done by k4, which means an additional volume control, dependent on bass and treble. Table 4–12 gives an application example for k10, k11 and k12 and Table 4–13 shows the dependence of k4/dB on bass and treble. In Table 4–14 the values for k4 corresponding to the dB values of Table 4–13 are listed. Fig. 4–5 shows the bass frequency response of every third step. The influence on the overall volume level, realized by VOL 1/2/3 is given in Table 4–9 and explained in the following.

As already mentioned in “Treble Adjustment”, treble boosting needs a correction of the overall volume level, which however is also dependent on the bass adjustment. Table 4–15 gives information on how to correct the overall volume according to the bass and treble status.

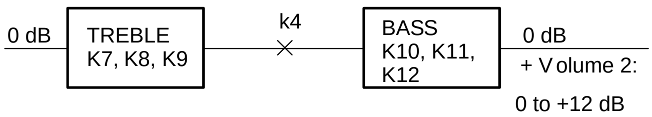


Fig. 4–3: Block diagram for bass and treble adjustment

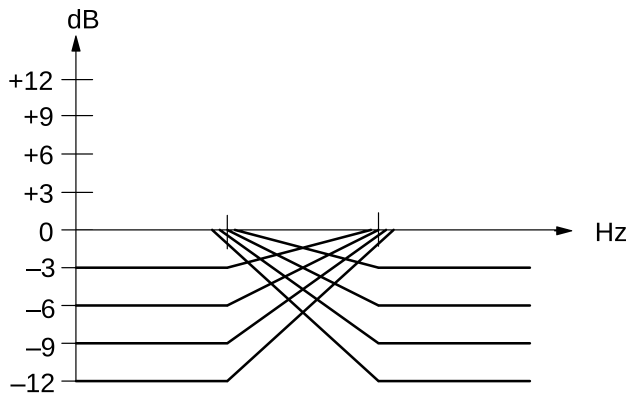


Fig. 4–4: Frequency response of the treble adjustment

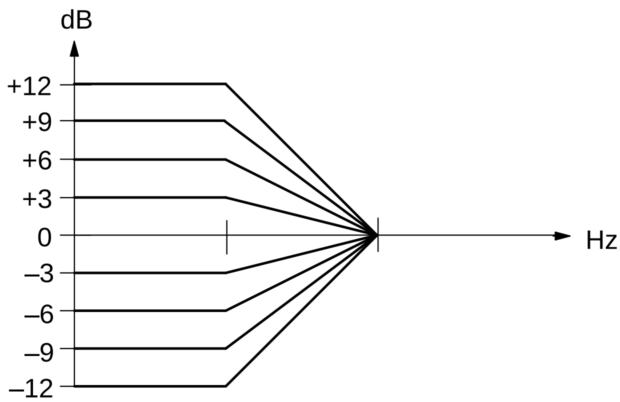


Fig. 4–5: Frequency response of the bass adjustment

Table 4–11: Coefficients for treble adjustment

Step/dB	Treble Coefficients (HEX and normalized) k7	k8	k9
+ 12	5B; 0.71	C0; –0.5	15; 0.16
+ 11	5F; 0.74	BE; –0.52	18; 0.19
+ 10	62; 0.77	BD; –0.52	1D; 0.23
+ 9	64; 0.78	BA; –0.55	29; 0.32
+ 8	68; 0.81	B8; –0.56	30; 0.38
+ 7	6B; 0.84	B7; –0.57	34; 0.41
+ 6	6F; 0.87	B3; –0.6	3B; 0.46
+ 5	70; 0.88	B8; –0.56	39; 0.45
+ 4	72; 0.89	BC; –0.53	37; 0.43
+ 3	75; 0.91	C2; –0.48	32; 0.39
+ 2	7A; 0.95	C8; –0.44	2D; 0.35
+ 1	7D; 0.98	D1; –0.37	28; 0.31
0	7F; 0.99	CO; –0.5	40; 0.5
– 1	73; 0.9	B5; –0.59	58; 0.69
– 2	69; 0.82	BF; –0.51	58; 0.69
– 3	62; 0.77	C6; –0.45	58; 0.69
– 4	56; 0.67	D2; –0.36	58; 0.69
– 5	50; 0.63	D8; –0.31	58; 0.69
– 6	48; 0.56	E0; –0.25	58; 0.69
– 7	42; 0.52	E6; –0.2	58; 0.69
– 8	3D; 0.48	EB; –0.16	58; 0.69
– 9	38; 0.44	F0; –0.13	58; 0.69
– 10	33; 0.4	F5; –0.09	58; 0.69
– 11	2F; 0.37	F9; –0.05	58; 0.69
– 12	2B; 0.34	FD; –0.02	58; 0.69

4.8.1. Example of Bass and Treble Adjustments

Increase of Bass and/or Treble (in 1 dB steps, see Tables 4–11 and 4–12)

1. set new value of k4 (Table 4–13)
2. set new set of k7, k8, k9 for bass or k10, k11, k12 for treble (Table 4–11 and 4–12)
3. adjust overall volume by means of Table 4–15:

find volume correction value (Table 4–15); increase the current volume level by this value in 1 dB steps (Table 4–9) and take the resulting values for VOL 1, VOL 2 and VOL 3, but keep the current k5 and store the former volume value. If the resulting volume value exceeds the maximum value (87), the difference from 87 should be stored. A later decrease of the volume value by means of the remote control unit could then cause the stored volume difference to be utilized.

Decreasing Bass and/or Treble (in 1 dB steps, see Tables 4–11 and 4–12)

1. set new set of k7, k8, k9 for bass or k10, k11, k12 for treble (Tables 4–11 and 4–12)
2. set new value of k4 (Table 4–13)
3. adjust overall volume by means of Table 4–15. This is to be done as described under “Increasing”, considering the difference of former and current volume correction values.

Table 4–12: Coefficients for bass adjustment

Step/dB	Bass Coefficients (HEX and normalized) k10	k11	k12
+ 12	7E; 0.98	8C; –0.91	7E; 0.98
+ 11	7F; 0.99	8C; –0.91	7D; 0.98
+ 10	7E; 0.98	8C; –0.91	7D; 0.98
+ 9	7F; 0.99	8C; –0.91	7C; 0.97
+ 8	7E; 0.98	8C; –0.91	7C; 0.97
+ 7	7F; 0.99	8C; –0.91	7B; 0.96
+ 6	7E; 0.98	8C; –0.91	7B; 0.96
+ 5	7F; 0.99	8C; –0.91	7A; 0.95
+ 4	7F; 0.99	8C; –0.91	79; 0.95
+ 3	7E; 0.98	8C; –0.91	79; 0.95
+ 2	7E; 0.98	8C; –0.91	78; 0.94
+ 1	7E; 0.98	8C; –0.91	77; 0.93
0	7F; 0.99	8C; –0.91	75; 0.91
– 1	7F; 0.99	8B; –0.91	75; 0.91
– 2	7F; 0.99	8A; –0.92	75; 0.91
– 3	7E; 0.98	8A; –0.92	75; 0.91
– 4	7E; 0.98	89; –0.93	75; 0.91
– 5	7E; 0.98	88; –0.94	75; 0.91
– 6	7E; 0.98	88; –0.94	74; 0.91
– 7	7D; 0.98	88; –0.94	75; 0.91
– 8	7D; 0.98	88; –0.94	74; 0.91
– 9	7C; 0.97	88; –0.94	75; 0.91
– 10	7C; 0.97	88; –0.94	74; 0.91
– 11	7C; 0.97	87; –0.95	75; 0.91
– 12	7C; 0.97	87; –0.95	74; 0.91

Table 4–13: Dependence of k4/dB on bass and treble

	Bass													
	dB	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0 . . .–12**	
	12	0	0	0	0	0	0	0	0	0	0	0	0	0	
	11	–1	0	0	0	0	0	0	0	0	0	0	0	0	
	10	–2	–1	0	0	0	0	0	0	0	0	0	0	0	
	9	–3	–2	–1	0	0	0	0	0	0	0	0	0	0	
	8	–4	–3	–2	–1	0	0	0	0	0	0	0	0	0	
T	7	–5	–4	–3	–2	–1	0	0	0	0	0	0	0	0	
	6	–6	–5	–4	–3	–2	–1	0	0	0	0	0	0	0	0
r	5	–7	–6	–5	–4	–3	–2	–1	0	0	0	0	0	0	
	4	–8	–7	–6	–5	–4	–3	–2	–1	0	0	0	0	0	
e	3	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	0	0	0	
	2	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	0	0	
b	1	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	0	
l	0	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
e	–1	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	–2	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	–3	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	–4	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	–5	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	0
	.	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	.	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	.	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	
	–12	–12	–11	–10	–9	–8	–7	–6	–5	–4	–3	–2	–1	0	

Table 4–14: Transfer table for k4

k4/dB	k4 Norm.	k4 HEX
–12	0.25	20
–11	0.28	24
–10	0.32	28
– 9	0.35	2D
– 8	0.4	33
– 7	0.45	39
– 6	0.50	40
– 5	0.56	48
– 4	0.63	51
– 3	0.71	5B
– 2	0.79	66
– 1	0.89	72
0	0.99	7F

The content of Table 4–13 can be expressed by the following logical expression:

IF [B > 0) and (B–T) > 0] THEN

IF [T ≥ 0] → k4/dB = T– B
IF [T < 0] → k4/dB = – B

ELSE

k4/dB = 0

END IF

T: Treble/dB;   B: Bass/dB

Table 4–15: Volume correction value (VCV) in dB (for bass < 0 dB all values = 0)

		Bass												
	dB	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**≤ 0**
	12	12	12	12	12	12	12	12	12	12	12	12	12	12
	11	12	11	11	11	11	11	11	11	11	11	11	11	11
	10	12	11	10	10	10	10	10	10	10	10	10	10	10
	9	12	11	10	9	9	9	9	9	9	9	9	9	9
	8	12	11	10	9	8	8	8	8	8	8	8	8	8
T	7	12	11	10	9	8	7	7	7	7	7	7	7	7
	6	12	11	10	9	8	7	6	6	6	6	6	6	6
r	5	12	11	10	9	8	7	6	5	5	5	5	5	5
	4	12	11	10	9	8	7	6	5	4	4	4	4	4
e	3	12	11	10	9	8	7	6	5	4	3	3	3	3
	2	12	11	10	9	8	7	6	5	4	3	2	2	2
b	1	12	11	10	9	8	7	6	5	4	3	2	1	1
l	0	12	11	10	9	8	7	6	5	4	3	2	1	0
e	–1	12	11	10	9	8	7	6	5	4	3	2	1	0
	–2	12	11	10	9	8	7	6	5	4	3	2	1	0
	–3	12	11	10	9	8	7	6	5	4	3	2	1	0
	–4	12	11	10	9	8	7	6	5	4	3	2	1	0
	–5	12	11	10	9	8	7	6	5	4	3	2	1	0
	.	12	11	10	9	8	7	6	5	4	3	2	1	0
	.	12	11	10	9	8	7	6	5	4	3	2	1	0
	.	12	11	10	9	8	7	6	5	4	3	2	1	0
	–12	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 4–15 can be expressed by the following logical expression, whereby T corresponds to the treble value in dB and B to the bass value in dB.

IF [B ≥ 0] OR [T>0] , then

IF [B > T] → VCV/dB = B
IF [B ≤ T] → VCV/dB = T

ELSE

VCV/dB = 0

END IF

4.9. Stereo Basewidth Enlargement SBE (only for Channel 1)

To simulate a larger stereo basewidth for TV receivers, audio signal components in the mid-frequency range are mixed from one channel into the other. As shown in Fig. 4–6, the corresponding components are subtracted from the L and the R channel. The coefficients for the bandpass filters are fixed and stored in the ACP's C-ROM. The basewidth enlargement can be switched on/off by means of coefficients k25 (see Table 4–16).

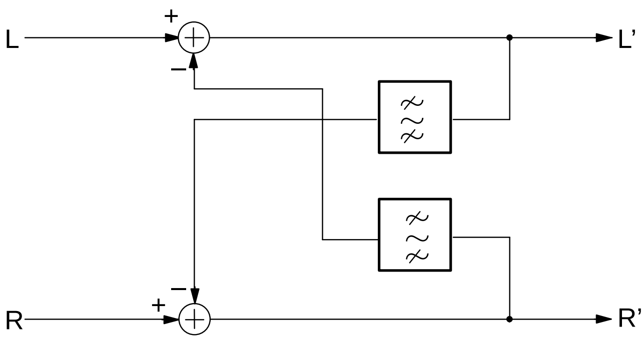


Fig. 4–6: Block diagram of stereo basewidth enlargement

Table 4–16: Switching of SBE

Operation Mode	**k26**
ON	80; –1.0
OFF	00; 0.0

4.10. Decoding of the Identification Signal

In the German TV standard, audio information can be transmitted in three modes: Mono, stereo or bilingual. To detect information about the current audio operation mode, the ACP has to detect the so-called identification signal, which can then be evaluated by the CCU. This signal, generated at the transmitter, is a peak at the identification frequency depending on the operation mode shown in Table 4–17, which modulates the amplitude of a pilot carrier. After addition to the R channel the resulting sum modulates the FM carrier. The pilot carrier frequency is 54.6875 kHz, which corresponds to 3.5 times the horizontal frequency.

Table 4–17: Identification frequencies for different operation modes

Operation Mode	Identification Frequency
Mono	none (=Pilot is unmodulated)
Stereo	117.5 Hz
Bilingual	274.1 Hz

To detect the identification signal, the ACP has theoretically to perform an amplitude demodulation, filtering and measurement of the level of the two possible identification frequencies. The CCU may then read these values for evaluation by its software. To manage this, the ACP 2371 NI uses a separate A/D converter (PDM3 and digital decimation filter). The digitized pilot signal is mixed in such a way, that the pilot falls to 475 Hz (at ΦM = 18.432 MHz). After decimation to a sampling rate of 2 kHz, amplitude demodulation of the signal is then performed.

A bandpass filter working in succession with three different coefficient sets (Table 4–18), which are supplied by the CCU, extracts the identification frequency (if available), rectifies and smooths out variations in the signal's level, receiving a value for the identification signal strength. This value (IDLEV) is then ready to be read by the CCU, where the evaluation is performed, assigning the correct center frequency of the respective bandpass to the corresponding level value.

It is obvious that the above bandpass filtering is a very critical item. The pass band has to be extremely narrow (0.32 Hz bandwidth) resulting in a high sensitivity of the center frequency to clock jitter. Therefore, for proper execution, the clock tolerance is expected to be in the range of ±400 ppm, i.e. a deviation of the bandpass center frequency of ±0.1 Hz.

4.10.1. Recommended Software Frame for Detection of the Identification Signal

The CCU software for the complete task should contain the items listed in Table 4–19, which have to be sequenced according to Table 4–20 or Table 4–21. Two cases must be distinguished in sequencing the items of Table 4–19:

1. After reset, program or channel change the sequence according to Table 4–20 has to be applied.

2. For further decoding of the identification signal the sequence of Table 4–21 is valid. Now after each IDLEV, which has been read from the ACP, evaluation is performed. Also the “ACP transient times” for the calculation of the IDLEVs is now extended, because now precise information about IDLEV is more important than very fast information, as is the case after reset, program or channel change.

The evaluation of **two** IDLEVs belonging to the two possible identification frequencies consists of their subtraction, and the difference being compared with a user-definable threshold level (TL) stored in the EAROM. TL should be approximately 10 hex.

To evaluate the IDLEVs, the two cases already mentioned have also to be considered:

1. After reset, program or channel change (= first decoding) → Current threshold level = ±0.5 · TL

2. For further decoding of the identification signal a hysteresis loop shown in Fig. 4–7 applies.

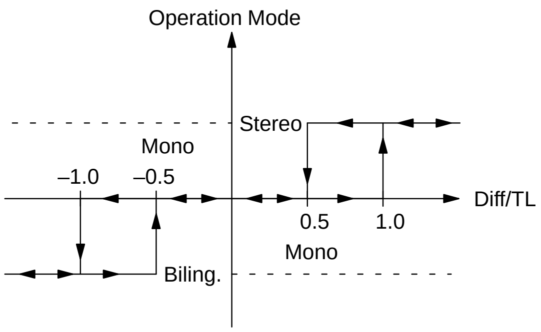


Fig. 4–7: Hysteresis loop for operation mode determination

Table 4–18: Coefficients transmitted between CCU and ACP, necessary for identification detection

Coefficient Set Direction	**Coefficient**	**Value HEX; Normalized**	**Comment**
BCS CCU to ACP	k27 k28 k29 k30 k03	38 ; 0.4375000 2F ; 0.3671875 7F ; 0.9921875 27 ; 0.3046875 7F ; 0.9921875	BCS = Bilingual Coefficient Set Set belongs to a center frequency of 274.1 Hz (= bilingual)
ICS CCU to ACP	k27 k28 k29 k30 k03	0 ; 0 0 ; 0 0 ; 0 81 ; –0.9921875 0 ; 0	ICS = Intermediate Coefficient Set
SCS CCU to ACP	k27 k28 k29 k30 k03	38 ; 0.4375000 29 ; 0.3203125 7F ; 0.9921875 6F ; 0.8671875 3E ; 0.4843750	SCS = Stereo Coefficient Set Set belongs to a center frequency of 117.5 Hz (= stereo)
Address 63 ACP to CCU	IDLEV	depending on operation mode	Calculated level to be evaluated by CCU

Note:
The sequence of coefficients must be: k27, k28, k29, k30, k03

Table 4–19: Instructions for mode identification

Item Name (arg)	**Comment**
TRANSF (CSET)	CCU transfers coefficient set BCS, ICS or SCS to ACP
WAIT (T)	CCU waiting cycle of T ms
FETCH (IDLEV)	CCU fetches IDLEV from ACP and memorizes it
EVALUATION	CCU evaluates last two IDLEVs, determining mono, stereo and bilingual

Table 4–20: Instruction sequence for case 1

Step	Item (arg)
1	TRANSF (ICS)
2	WAIT (T > 1)
3	TRANSF (BCS)
4	WAIT (750)
5	FETCH (IDLEV)
6	TRANSF (ICS)
7	WAIT (T > 1)
8	TRANSF (SCS)
9	WAIT (750)
10	FETCH (IDLEV)
11	EVALUATION

4.11. ACP 2371 NI Initialization

After switching on the power, or after reset, the ACP 2371 NI requires a certain startup time (Fig. 4–8) to accept coefficients and valid audio data.

– Immediately after a reset, the VOL 1 (k0/1) is automatically set to zero

– After a delay of another 0.5 s (or 0.6 s after power-on), a complete set of coefficients is transferred by the CCU via the IM bus, beginning with the Select Register Coefficient (Addr. 102) and keeping VOL 1 zero.

– 20 ms later, the mute function is switched off by the CCU

To transfer a complete set of coefficients to the ACP the following sequence is recommended:

1. Select register for processor selection
2. k33,k32,k35,k37 control words for standard selection of mode, analog input and gain
3. k13, k23–k25 DSP input select
4. Identification decoding: k27 to k30, k03
5. Dematrixing coefficients: k14 to k22 for mono
6. Bass and treble coefficients: k4, k7 to k12
   If not corresponding to 0 dB, k4 and volume value have to be calculated to be considered in mute off.
7. Remaining unset coefficients except volume

Table 4–21: Instruction sequence for case 2

Step	Item (arg)
1	TRANSF (ICS)
2	WAIT (T > 1)
3	TRANSF (BCS)
4	WAIT (2000)
5	FETCH (IDLEV)
6	EVALUATION
7	TRANSF (ICS)
8	WAIT (T > 1)
9	TRANSF (SCS)
10	WAIT (2000)
11	FETCH (IDLEV)
12	EVALUATION

8. Mute off. Switching to mute off should be done as described in section 4.6.

Note: The maximum IM bus transfer rate must not exceed the sampling frequency (32 kHz).

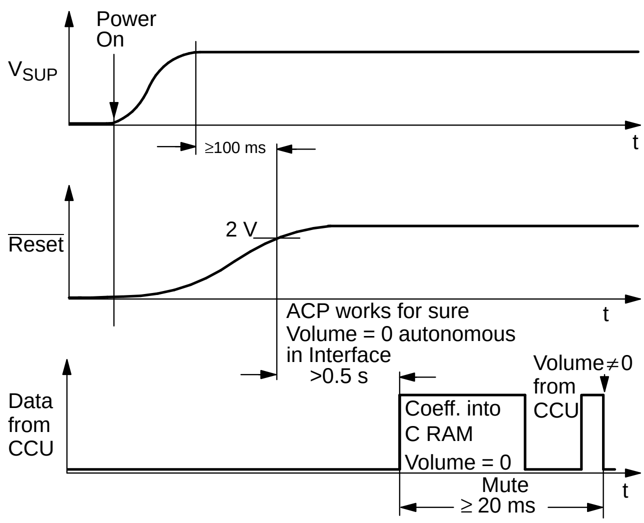


Fig. 4–8: Initialization of the ACP 2371 NI

4.12. Complete Coefficient Table

Table 4–22 details all coefficients and control words which can be influenced by the CCU. The chapters containing more details about certain coefficients are noted in the right-hand column.

Table 4–22: Available addresses in the ACP C-RAM and their applications

Address	Coefficient	Description	See Section
Value to be read from the ACP's Output Buffer to the CCU			
63	IDLEV	Identification Signal Strength	(4.10.)
Values to be written into the ACP's C-RAM			
64 65 66	k00 k01 k02	Balance · Volume = VOL 1 R Channel 1 Balance · Volume = VOL 1 L Channel 1 VOL 3 Channel 1	(4.6.) (4.6.) (4.6.)
67 68 69 70	k03 k04 k05 k06	Coeff. for Identification Filter Bass Level Correction Loudness Intensity VOL 4 Channel 2	(4.10.) (4.8.) (4.7.) (4.6.)
71 72 73	k07 k08 k09	Coefficient for Treble Filter Coefficient for Treble Filter Coefficient for Treble Filter	(4.8.) (4.8.) (4.8.)
74 75 76	k10 k11 k12	Coefficient for Bass Filter Coefficient for Bass Filter Coefficient for Bass Filter	(4.8.) (4.8.) (4.8.)
77	k13	Input Select Channel 2: NICAM / FM	(4.3.)
78 79 80 81	k14 k15 k16 k17	Dematrixing Channel 1 Dematrixing Channel 1 Dematrixing Channel 1 Dematrixing Channel 1	(4.4.) (4.4.) (4.4.) (4.4.)
82	k18	FM-Deemphasis	(4.2.)
83 84 85 86	k19 k20 k21 k22	Dematrixing Channel 2 Dematrixing Channel 2 Dematrixing Channel 2 Dematrixing Channel 2	(4.4.) (4.4.) (4.4.) (4.4.)
87 88 89	k23 k24 k25	Input Select Channel 1: PDM Input Select Channel 1: FM Input Select Channel 1: NICAM	(4.3.) (4.3.) (4.3.)
90	k26	Basewidth Enlargement	(4.9.)
91 92 93 94	k27 k28 k29 k30	Coefficient for Identification Filter Coefficient for Identification Filter Coefficient for Identification Filter Coefficient for Identification Filter	(4.10.) (4.10.) (4.10.) (4.10.)
95	k31	SW-Conversion Filter	(4.2.)
96 97	k32 k33	Switch S1 to S5; DOUT; Clock Divider; AUXOUT Mute Control Word for Standard Selection	(2.1.), (2.7) (Note 2)
98	k34	VOL 2 Analog Volume Control Channel 1	(4.6.1.)
99 101	k35 k37	Additional Gain Adjustment of TVIN2; Switch S1, S6, S7 Level Control; Switch S3	(2...) (2.4.)
102	Select Register	Processor Selection	(3.1.3.2.)
103	k39	VOL 5 Analog Volume Control Channel 2	(4.6.2.)

Note to Table 4–22:

Cascading of two or more ACPs for future applications requires additional control information concerning the S bus. This is done by means of k33, and to ensure upward compatibility all bits are defined as follows:

k33:	Bit 7	=	0 *	clock divider = 4; ΦPDM = ΦM: 4 (section 3.3.)
		=	1	clock divider = 3; ΦPDM = ΦM: 3 (section 3.3.)
	Bit 6	=	0 *	sampling rate is derived from system clock (section 3.3.)
		=	1	sampling clock according to SIDENT of digital source (S bus) (section 3.3.)
	Bit 5	=	0 *	normal mode
		=	1	test mode

concerning the S bus the ACP 2371 NI is:

Bit 4	=	0 *	S bus slave
	=	1	S bus master (the ACP 2371 NI generates SCLK and SIDENT)
Bit 3	=	0	S bus data output active
	=	1 *	S bus data output = high impedance
Bit 2	=	0 *	Pal mode (sampling rate = ΦPDM : 128) (section 3.3.)
	=	1	D2MAC/NICAM mode (sampling rate = ΦPDM :144) (section 3.3.)
Bit 1	=	0 *	normal S bus input
	=	1	S bus access to conversion filter
Bit 0	=	0	not used, for compatibility must be set to 0.

*) Reset status.

5. Specifications

5.1. Outline Dimensions

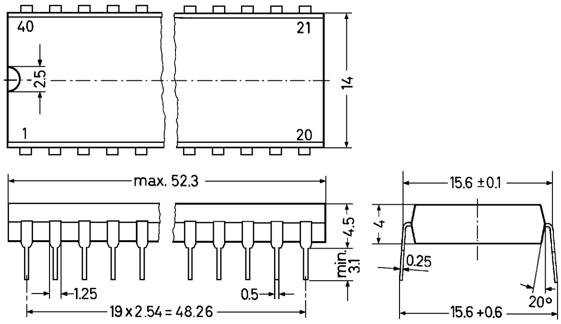


Fig. 5–1: ACP 2371 NI in 40-pin DIL Package
Weight approx. 6 g   Dimensions in mm

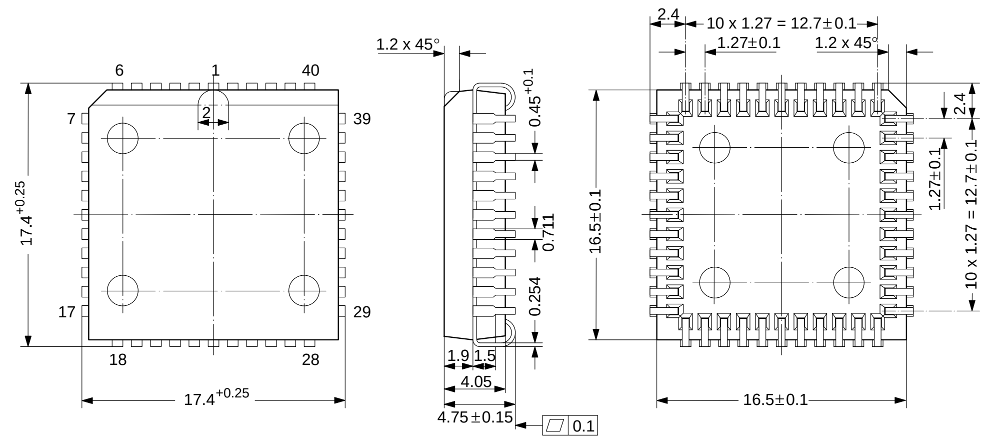


Fig. 5–2: ACP 2371 NI in 44-pin PLCC Package
Weight approx. 2.2 g   Dimensions in mm

5.2. Pin Connections

5.2.1. 40-Pin DIL Package

1	VSUP
2	GND
3	SCLK
4	SDAT
5	$\overline{\text{RESET}}$
6	ΦM
7	SID
8	DOUT
9	VSUP
10	AUXDIN1
11	AUXDIN2
12	AUXIN1
13	AUXIN2
14	TVIN1
15	Leave Vacant
16	TVIN2
17	PILOTIN
18	VSUP ANALOG
19	GND ANALOG
20	VREF

21	VA
22	PDMC1
23	PDMC2
24	PDMC3
25	BAI
26	DE12
27	DE11
28	AUXOUT1
29	AUXOUT2
30	DAC2L
31	DAC2R
32	IREF1
33	DAC1L
34	DAC1R
35	GND ANALOG
36	IREF2
37	IMDAT
38	IMID
39	IMCL
40	SOUT

5.2.2. 44-Pin PLCC Package

1	VSUP
2	GND
3	GND
4	SCLK
5	SDAT
6	$\overline{\text{RESET}}$
7	ΦM
8	SID
9	DOUT
10	$\overline{\text{PDM1}}$
11	$\overline{\text{PDM2}}$
12	VSUP
13	AUXDIN1
14	AUXDIN2
15	AUXIN1
16	AUXIN2
17	TVIN1
18	TVIN2
19	PILOTIN
20	VSUP ANALOG
21	GND ANALOG
22	VREF
23	VA
24	PDMC1
25	PDMC2
26	PDMC3
27	BAI
28	DE12
29	DE11
30	AUXOUT1
31	AUXOUT2
32	DAC2L
33	DAC2R
34	IREF1
35	DAC1L
36	DAC1R
37	GND ANALOG
38	IREF2
39	IMDAT
40	GND

41	IMID
42	IMCL
43	SOUT
44	VSUP

5.3. Pin Descriptions (pin numbers for 44-pin PLCC package)

Pins 1, 12, 44 – VSUP: Digital Supply Voltage
These pins must be connected to the positive supply.

Pins 2, 3, 40 – GND: Digital Ground, 0 V
These pins must be connected to the negative supply. They have to be used for ground connections in conjunction with digital signals.

Pins 4, 5, 8, 43 – Serial Audio Interface (S Bus)
Pins 4 SCL and 8 SID are S-Clock and S-Ident inputs/outputs (Fig.5–9), the status depending on bit 4 in coefficient k33. Pin 5 SDIN is the S-Data input (Fig. 5–7) and pin 43 SDOUT the S-Data output (Fig. 5–10)

Pin 6 – $\overline{\text{RESET}}$: Reset Input (Fig. 5–4)
In the steady state, high level is required at pin 6. A low level resets the ACP 2371. Initialization of the ACP 2371 NI is described in section 4.11.

Pin 7 – ΦM: Main Clock Input (Fig. 5–5)
This pin receives the required main clock signal from the MCU 2600 Clock Generator IC or from the DMA 2271 D2-MAC Decoder or the MSP 2410 NICAM Demodulator/Decoder.

Pin 9 – DOUT: Data Output (Fig. 5–12)
This output provides the status of bit 6 (IM Bus address = 60 HEX).
Bit 6 = 0 $\rightarrow$ Pin 9 = 0
Bit 6 = 1 $\rightarrow$ Pin 9 = 1

Pins 10, 11 – $\overline{\text{PDM1}}$ and $\overline{\text{PDM2}}$: Digital Inputs/Outputs 1 and 2 (Fig. 5–6)
These pins either receive the pulse-density modulated output signals of the ADC 2301E or ADC 2311E, or serve as outputs of the pulse-density modulators PDM1 and PDM2 controlled by the switch S6.

Pins 13, 14 – AUXDIN1, AUXDIN2: Second Auxiliary Analog Inputs 1 and 2 (Fig. 5–15)
These inputs can be used for additional sources like D2MAC or NICAM and provide an easy interface to the auxiliary outputs (Pins 30 and 31) with no need of external switches.

Pins 15, 16 – AUXIN1, AUXIN2: Auxiliary Inputs 1 and 2 (Fig. 5–15)
These inputs can be used as playback Inputs from a video recorder or other external sources. The input signals must be coupled via capacitors. The input signal range can be expanded by adding series resistors.

Pins 17, 18 – TVIN1, TVIN2: TV Audio Inputs 1 and 2 (Fig. 5–15)
These two inputs receive their input signals from the sound demodulator of the TV set. These signals must be coupled via capacitors.

Pin19 – PILOTIN: Analog (TV) Pilot Input (Fig. 5–15)
It is possible to supply the ACP 2371 NI with the pilot signal. This signal must be coupled via a capacitor.

Pin 20 – VSUP ANALOG: Analog Supply Voltage
Power is supplied via this pin for the analog circuitry of the ACP 2371.

Pins 21, 37 – GND ANALOG: Analog Ground, 0 V
These pins serve as ground connection for the analog signals.

Pin 22 – VREF: Analog Ground, 0 V
The same as pins 21 and 37, this pin must also be connected separately to the single ground point. It serves as a ground connection for the analog bias circuits.

Pin 23 – VA: Internal Ground, d.c. level = +2.25 V
This pin serves as the internal ground connection for the analog circuitry. It must be connected to Analog Ground with a 3.3 μF and a 100 nF capacitor in parallel.

Pins 24, 25, 26 – PDMC1, PDMC2, PDMC3: Capacitor Connections
The filter capacitors for the outer feedback loops of the pulse-density modulators PDM1, PDM2 and PDM3 must be connected between these pins and pin 27.

Pin 27 – BAI: Buffered Internal Ground, d.c. level = +2.25 V
This pin is the buffered internal ground connection for the external capacitors connected to pins 24, 25, 26, 28 and 29.

Pin 28 – DE12: Capacitor Connection
This pin serves to connect the second deemphasis capacitor. The signal at this pin is the second TV sound channel (2R).

Pin 29 – DE11: Capacitor Connection
The first deemphasis capacitor must be connected to this pin. Depending on the state of the analog switch S2, the signal at this pin is either the first TV sound channel or the dematrixed 2L signal.

Pin 30 and 31 – AUXOUT1, AUXOUT2: Auxiliary Analog Outputs 1 and 2 (Fig. 5–13)
These analog outputs provide either the signals of the TV inputs pin 17 and 18 or the signals of the auxiliary analog input pins 13 and 14 according to the state of the analog switch S3 which is set via the IM bus, see section 2.1.

Pins 32, 33 – DAC2L, DAC2R: DAC Outputs 2L and 2R (Fig. 5–11)
These pins supply the audio output signals as output currents whose amplitudes are determined by the reference current IREF2 fed to pin 38. The output signals of pins 32 and 33 are influenced by the VOL4 and VOL5 volume control facilities.

Pins 34, 38 –IREF1, IREF2: Reference Current Inputs (Fig. 5–3)
These Inputs require a current of 150 µA called reference current Iref. They serve for volume adjustment in the DAC interfaces.

Pins 35, 36 – DAC1L, DAC1R: DAC Outputs 1L and 1R (Fig. 5–11)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current Iref1 fed to pin 34. The output signals of pins 35 and 36 are influenced by the VOL1, VOL2 and VOL3 volume control facilities.

Pins 39, 41 and 42 – IMDAT, IMID, IMCL: IM Bus Connections
Via these pins, the APU 2371 is connected to the IM bus and communicates with the CCU. Pins 41 (IM Bus Ident input) and 42 (IM Bus Clock input) have the configuration shown in (Fig. 5–4). Pin 39 (IM Bus Data input/output) is shown in (Fig. 5–8). The IM bus is described in section 3.1.3.1.

5.4. Pin Circuits (pin numbers for 44-pin PLCC package)

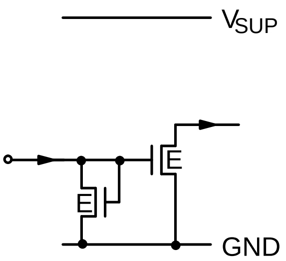


Fig. 5–3:
Input Pins 34, 38

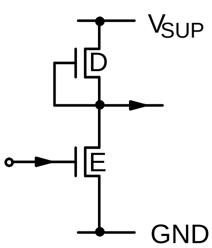


Fig. 5–4:
Input Pins 6, 41, 42

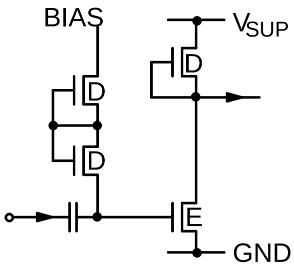


Fig. 5–5:
Input Pin 7

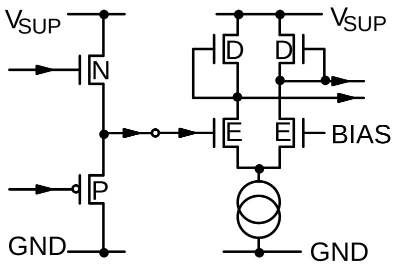


Fig. 5–6:
Input/Output Pins 10, 11

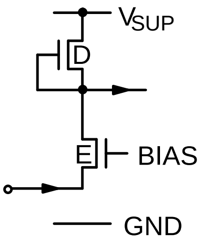


Fig. 5–7:
Input Pin 5

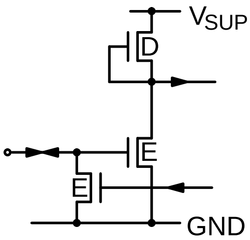


Fig. 5–8:
Input/Output Pin 39

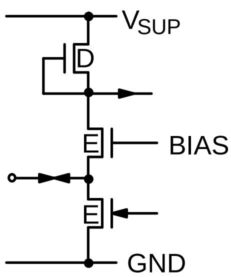


Fig. 5–9:
Input/Output Pins 4, 8

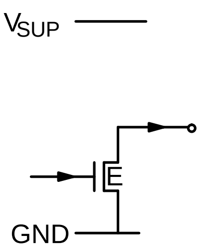


Fig. 5–10:
Output Pin 43

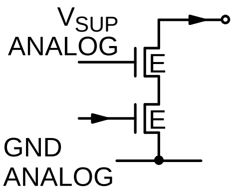


Fig. 5–11:
Output Pins 32, 33, 35, 36

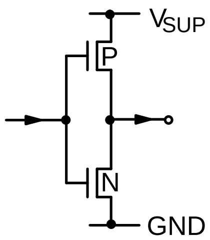


Fig. 5–12:
Output Pin 9

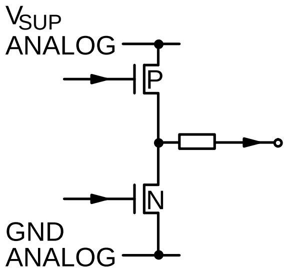


Fig. 5–13:
Output Pins 30, 31

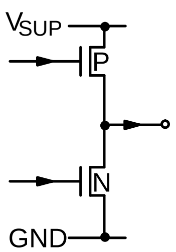


Fig. 5–14:
Output Pin 27

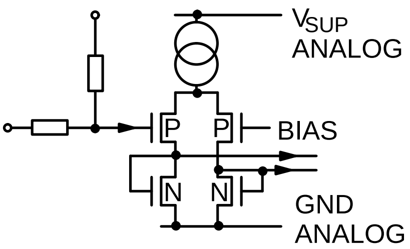


Fig. 5–15:
Input Pins 13–19

5.5. Electrical Characteristics (pin numbers for 44-pin PLCC package)

(All voltages refer to pins 2, 3, 21, 37 and 40).

5.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	1, 12, 20, 44	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUP}	–
V_O	Output Voltage	10, 11, 24 to 26, 28 to 31	–0.3 V	V_{SUP}	–
V_{DO}	DAC Output Voltage	32, 33, 35, 36	–0.3	+12	V
V_{SDO}	S-Bus Output Voltage	4, 8, 43	–0.3 V	V_{SUP}	–
I_{SDO}	DAC and S-Bus Output Current	4, 8, 32, 33, 35, 36, 43	–	10	mA
I_{IMO}	IM Bus Output Current	39	–	*	mA
I_{BAIO}	BAI Output Current	27	–	10	µA

* This output is short-circuit proof with respect to supply and ground

5.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	1, 12, 20, 44	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	7	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$	–
V_{REIL}	Reset Input Low Voltage	6	–	–	1.2	V
V_{REIH}	Reset Input High Voltage		2.4	–	–	V
I_{REF}	Reference Input Current	34, 38	–	0.15	–	mA
V_{DACB}	DAC D.C. Bias Voltage	32, 33, 35, 36	5	–	–	V

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{TVINI}	TVIN Input Voltage, RMS*) at Level Control ON at Level Control OFF	17, 18	 – –	 – –	 1.0 0.5	 V V
V_{AUXINI}	AUXIN Input Voltage, RMS*) at Level Control ON at Level Control OFF	15, 16	 – –	 – –	 1.0 0.5	 V V
$V_{AUXDINI}$	AUXDIN Input Volt., RMS*) at Level Control ON at Level Control OFF	13, 14	 – –	 – –	 1.0 0.5	 V V
V_{DE1I}	DE1 Input Voltage, RMS*)	28, 29	–	–	0.26	V
$V_{PILOTINI}$	PILOTIN Input Voltage, RMS*) at 54.7 kHz	19	15	20	60	mV
R_G	Source Resistance for all Analog Inputs	13 to 19	–	–	10	kΩ
C_{PDM}	PDM Capacitor	24, 25, 26	–5%	680	+5%	pF
V_{IMIL}	IM Bus Input Low Voltage	39, 41, 42	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End-Pulse Input		6.0	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End-Pulse Low Time		3.0	–	–	µs

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SIL}	Sound Bus Input Low Voltage	4, 5, 8	–	–	0.4	V
$-I_{SIH}$	Sound Bus Input High Current		–	–	20	µA
f_{IS}	ΦS Sound Clock Input Frequency	4	–	$\frac{f_{\Phi M}}{4}$	–	–
$\frac{t_{S2}}{t_{S1}}$	ΦS Clock Input High/Low Ratio		0.8	1	1.2	–
t_{S3}	ΦS Clock Input Setup Time before Ident End-Pulse Input	4, 8	150	–	–	ns
t_{S4}	Sound Bus Data Input Setup Time before ΦS Clock Input	4, 5	50	–	–	ns
t_{S5}	Sound Bus Data Input Hold Time after ΦS Clock Input		50	–	–	ns
t_{S6}	Sound Bus Ident End-Pulse Input Low Time	8	150	–	–	ns
*) These values apply for a crest factor of 1.414 only (e.g. sinewave).						

5.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	1+12 +20+44	–	150	180	mA	
V_{IMOL}	IM Bus Output Low Voltage	39	–	–	0.4	V	I_{IMO} = 3 mA
I_{IMOH}	IM Bus Output High Current		–	–	10	µA	V_{IMO} = 5 V
$-I_{SIL}$	S-Clock/Ident/Data Input Low Current	4, 5, 8	–	1	2.7	mA	V_{SI} = 0.3 V
V_{SIH}	S-Clock/Ident/Data Input High Voltage		–	–	1.2	V	I_{SI} = 0
V_{SOL}	S-Bus Output Low Voltage	4, 5, 43	–	–	0.3	V	I_{SO} = 6 mA
I_{SOH}	S-Data Output High Current	43	–	–	10	µA	V_{SO} = 5 V
R_i	Input Resistance TVIN Inputs AUXIN Inputs AUXDIN Inputs PILOTIN Input	 17, 18 15, 16 13, 14 19	34 24	50 35	70 49	kOhm kOhm	 Level Control OFF Level Control OFF Level Control OFF
$R_{AUXOUTO}$	AUXOUT Output Resistance	30, 31	525	750	975	Ohm	
$V_{AUXOUTB}$	AUXOUT Output DC Bias Voltage		–	2.25	–	V	
R_{DE1}	Internal DE1 Resistors	28, 29	– –	3.5 15	– –	kOhm kOhm	DE1 ON, Mute OFF DE1 ON, Mute ON

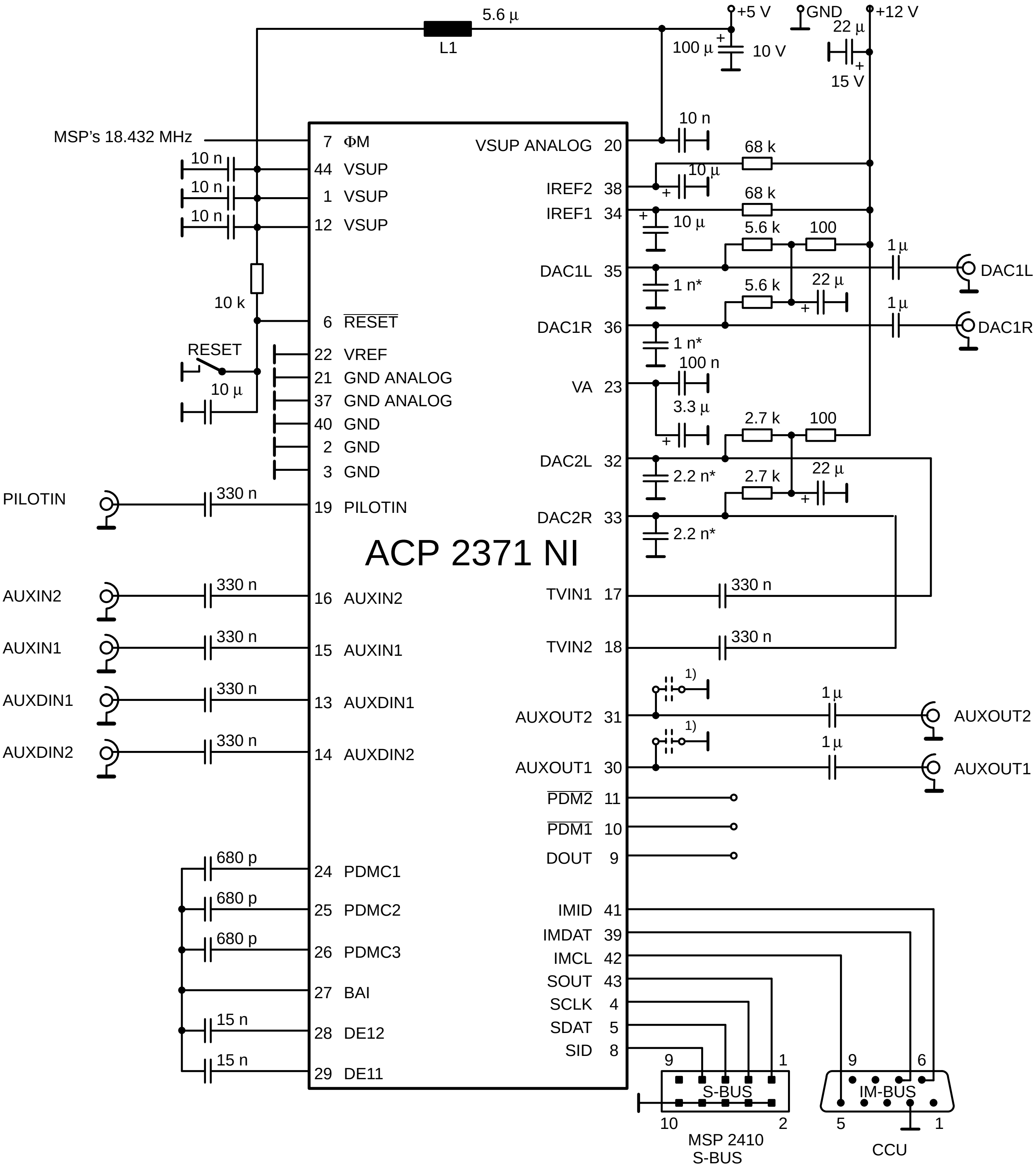
Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
THD+N	Total Harmonic Distortion plus Noise						unweighted, BW = 15 kHz, Signal = 1kHz at V_{IN} = 350mV RMS or –3 dB Full Digital Scale, level control off
	AUXIN to DAC1	15, 16; 35, 36	–	0.06	0.08	%	
	AUXDIN to DAC1	13, 14; 35, 36	–	0.06	0.08	%	
	SBUS to DAC1	35, 36	–	0.06	0.08	%	
	SBUS to DAC2	32, 33	–	0.06	0.08	%	
	TVIN to AUXOUT	17, 18; 30, 31	–	0.02	0.03	%	
	AUXIN to AUXOUT	15, 16; 30, 31	–	0.02	0.03	%	
	AUDIN to AUXOUT	13, 14; 30, 31	–	0.02	0.03	%	
SNR	Signal to Noise Ratio						RMS, unweighted, BW = 15 kHz , Signal = 1kHz at V_{IN} = 0.5 V RMS or 0 dB Full Digital Scale, noise measurement with signal at –20 dB, 1 kHz
	AUXIN to DAC1	15, 16; 35, 36	80	82	–	dB	
	AUXDIN to DAC1	13, 14; 35, 36	80	82	–	dB	
	SBUS to DAC1	35, 36	80	82	–	dB	
	SBUS to DAC2	32, 33	80	82	–	dB	
	TVIN to AUXOUT	17, 18; 30, 31	80	82	–	dB	
	AUXIN to AUXOUT	15, 16, 30, 31	80	82	–	dB	
	AUXDIN to AUXOUT	13, 14, 30, 31	80	82	–	dB	
G	Gain						
	AUXIN to DAC 1	15, 16; 35, 36	1.8	2.0	2.2	–	
	AUXDIN to DAC 1	13, 14; 35, 36	1.8	2.0	2.2	–	
	TVIN to AUXOUT	17, 18; 30, 31	1.8	2.0	2.2	–	
	AUXIN to AUXOUT	15, 16; 30, 31	1.8	2.0	2.2	–	
	AUXDIN to AUXOUT	13, 14; 30, 31	1.8	2.0	2.2	–	
	Stereo Separation by Dematrix		30	–	–	dB	
CA	Crosstalk Attenuation within Active Channel Pair		55	60	–	dB	test input V_{IN} = 0.5 V RMS, 1 kHz all other inputs 1 KOhm to ground, level control off
	from non–selected Input		75	–	–	dB	

Characteristics, continued

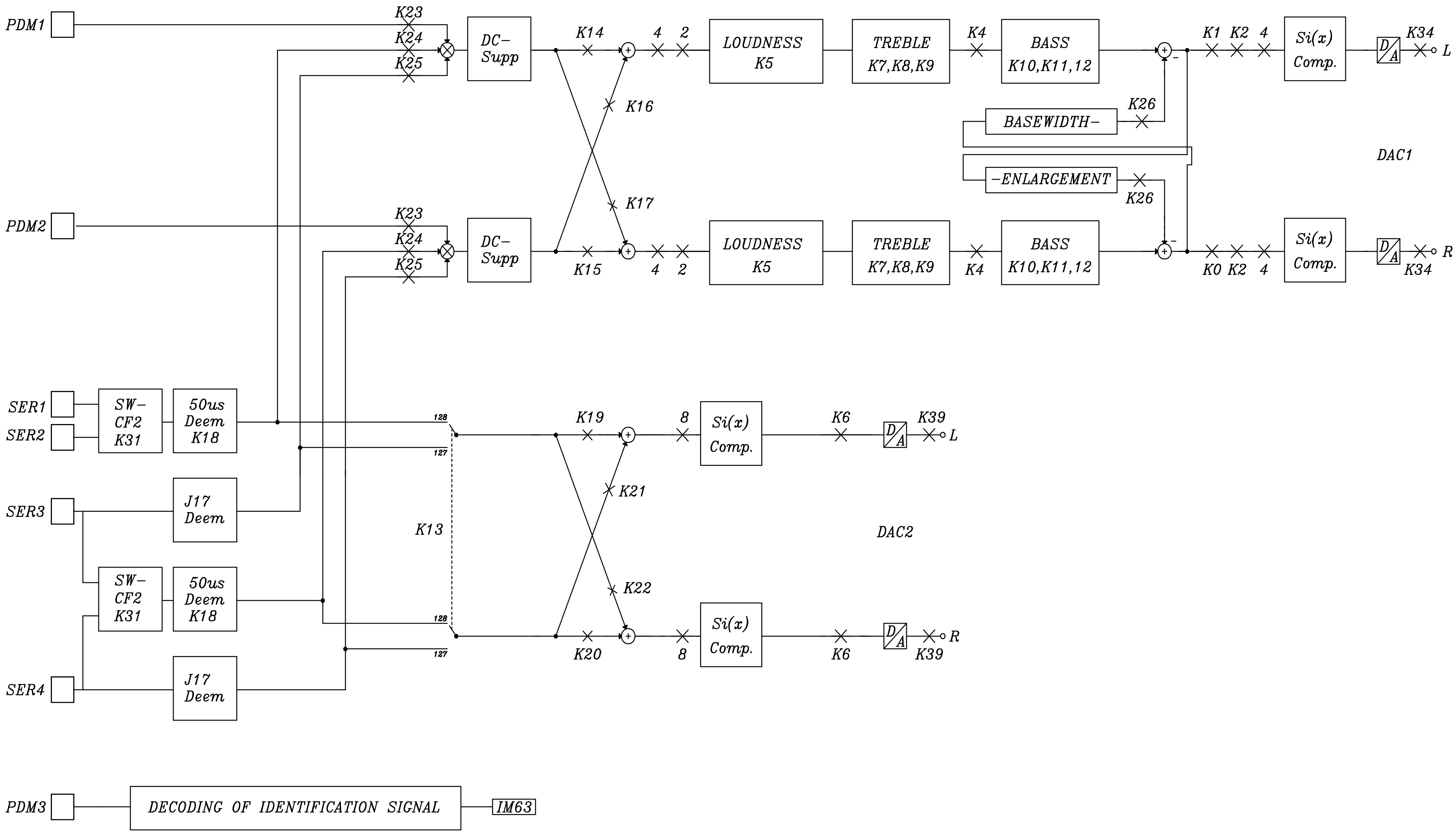
Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
	Input Level, RMS, for PDM Clipping* TVIN and AUXIN	15, 16, 17, 18	500	550	600	mV	Level Control OFF
	Margin to PDM Clipping Level		0	10	20	%	at TVIN or AUXIN = 600 ... 1.0 V, Level Control On
V_{PDMH}	PDM High Level	10, 11	0.5 $\cdot V_{SUP}$ –0.3 V	–	–	–	at C_L = 20 pF
V_{PDML}	PDM Low Level		–	–	0.5 $\cdot V_{SUP}$ –0.3 V		at C_L = 20 pF
V_{DOUTOH}	Data Output High Level	9	–	3.7	–	V	No Load
V_{DOUTOL}	Data Output Low Level		–	0.4	0.5	V	No Load
R_{DOUTO}	Data Output Output Resistance		–	2	–	kOhm	
	IDLEV Value	39	32	40	50	dec	at 20 mV on PILOTIN
I_{DAC1O}	DAC1 Output Peak-to-peak Current	35, 36	–	0.81	–	mA	I_{REF1} = 0.15 mA, VOL2 = 0 dB
			–	25	–	µA	I_{REF1} = 0.15 mA, VOL2 = –30 dB
I_{DAC2O}	DAC2 Output Peak-to-peak Current	32, 33	–	0.81	–	mA	I_{REF2} = 0.15 mA, VOL5 = 0 dB
			–	25	–	µA	I_{REF2} = 0.15 mA, VOL5 = –30 dB
V_{REF1}	Reference Input1 Voltage Drop	34	–	2.5	–	V	R_{REF1} = 68 kOhm from +12 V, VOL2 = 0 dB
			–	0.45	–	V	R_{REF1} = 68 kOhm from +12 V, VOL2 = –30 dB
V_{REF2}	Reference Input2 Voltage Drop	38	–	2.5	–	V	R_{REF2} = 68 kOhm from +12 V, VOL5 = 0 dB
			–	0.45	–	V	R_{REF2} = 68 kOhm from +12 V, VOL5 = –30 dB

6. Appendix 1: Application Circuit (pin numbers for 44-pin PLCC package)



* Capacitors = 5%; all resistors = 1%; 1) see section 2.5.

7. Appendix 2: Program Structure of the ACP 2371NI



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