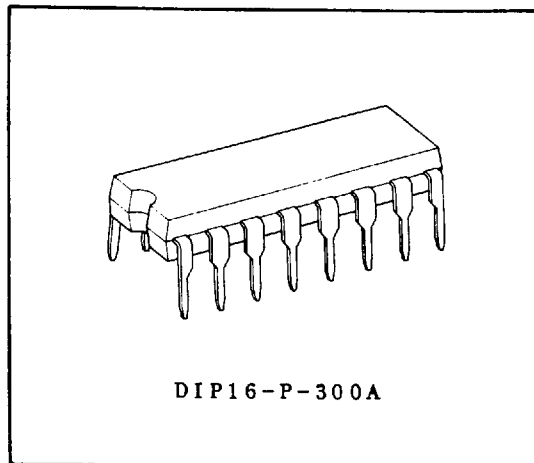


3V DUAL PRE AMPLIFIER + HEADPHONE DRIVER SYSTEM IC

The TA8111AP is consisted all of playback circuits (pre amp + headphone driver) for the 3V stereo headphone tape player.

The pre amplifier is independent of the headphone driver which loop voltage gain is fixed at 36dB.

- . Operation Supply Voltage : $V_{CC}=1.8\sim 6.0V$ ($T_a=25^\circ C$)
- . Built-in Ripple Filter Terminal
- . Input Condenser-less for Pre Amplifier



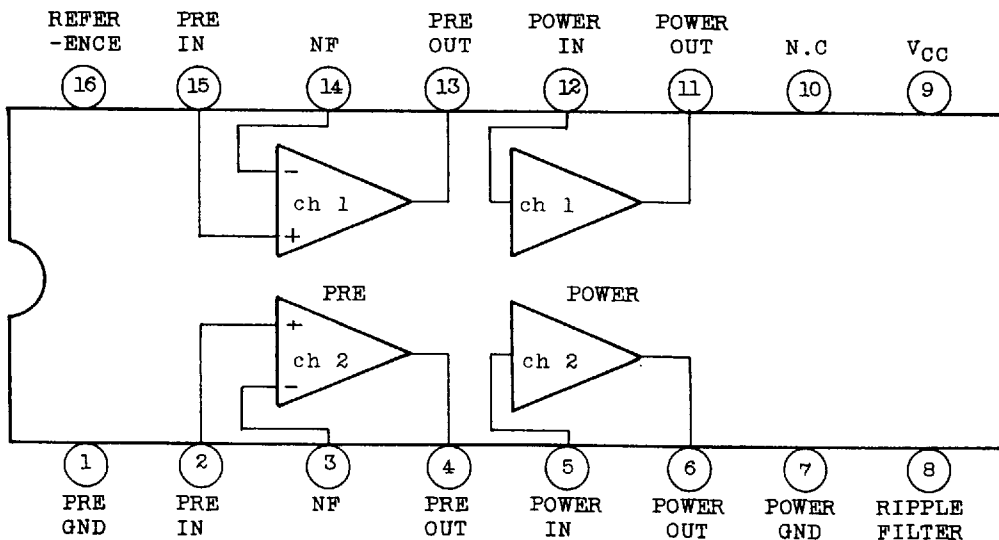
Weight: 1.0g(Typ.)

MAXIMUM RATINGS ($T_a=25^\circ C$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	6	V
Power Dissipation (Note)	P_D	750	mW
Operating Temperature	T_{opr}	-25~75	$^\circ C$
Storage Temperature	T_{stg}	-55~150	$^\circ C$

Note: Derated above $T_a=25^\circ C$ in the proportion of 6mW/ $^\circ C$.

BLOCK DIAGRAM



9097247 0020161 797

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TA8111AP-1
1991-9-18
TOSHIBA CORPORATION

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $V_{CC}=3V$, $f=1kHz$, $R_L=32\Omega$, (PW section), NAB circuit, $T_a=25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{CCQ}		$V_{in}=0$, $R_g=2.2k\Omega$	-	9	16	mA

(PRE AMPLIFIER SECTION)

Open Loop Voltage Gain	G_{VO}		$V_{OUT}=-10dBm$	66	76	-	dB
Total Harmonic Distortion	THD		$V_{OUT}=-10dBm$, NAB33dB	-	0.03	0.1	%
Maximum Output Voltage	V_{OM}		THD=1%	300	450	-	mV _{rms}
Equivalent Input Noise Voltage	V_{NI}		$R_g=2.2k\Omega$, BW= ~20kHz NAB=1k Ω	-	0.9	1.5	μV_{rms}
Ripple Rejection Ratio	R.R		$f_{rip}=100Hz$, $R_g=2.2k\Omega$ $V_{rip}=-10dBm$, NAB33dB	45	55	-	dB
Input Bias Current	I_B		$V_{in}=0$	-	0.5	1.5	μA

(POWER AMPLIFIER SECTION)

Output Power	P_{OUT1}		THD=10%, $R_L=32\Omega$	27	38	-	mW
	P_{OUT2}		THD=10%, $R_L=16\Omega$	-	50	-	
Closed Loop Voltage Gain	G_V		$V_{OUT}=-10dBm$	33	36	39	dB
Total Harmonic Distortion	THD1		$P_{OUT}=1mW$, $R_L=32\Omega$	-	0.6	2.0	%
	THD2		$P_{OUT}=1mW$, $R_L=16\Omega$	-	1.0	-	
Output Noise Voltage	V_{NO}		$R_g=600\Omega$, BW=~20kHz	-	80	160	μV_{rms}
Ripple Rejection Ratio	R.R		$f_{rip}=100Hz$, $R_g=600\Omega$ $V_{rip}=-10dBm$	44	63	-	dB
Input Resistance	R_{IN}			15	20	-	k Ω
Input Bias Current	I_B		$R_g=100k\Omega$, $V_{in}=0$	-	5	40	nA

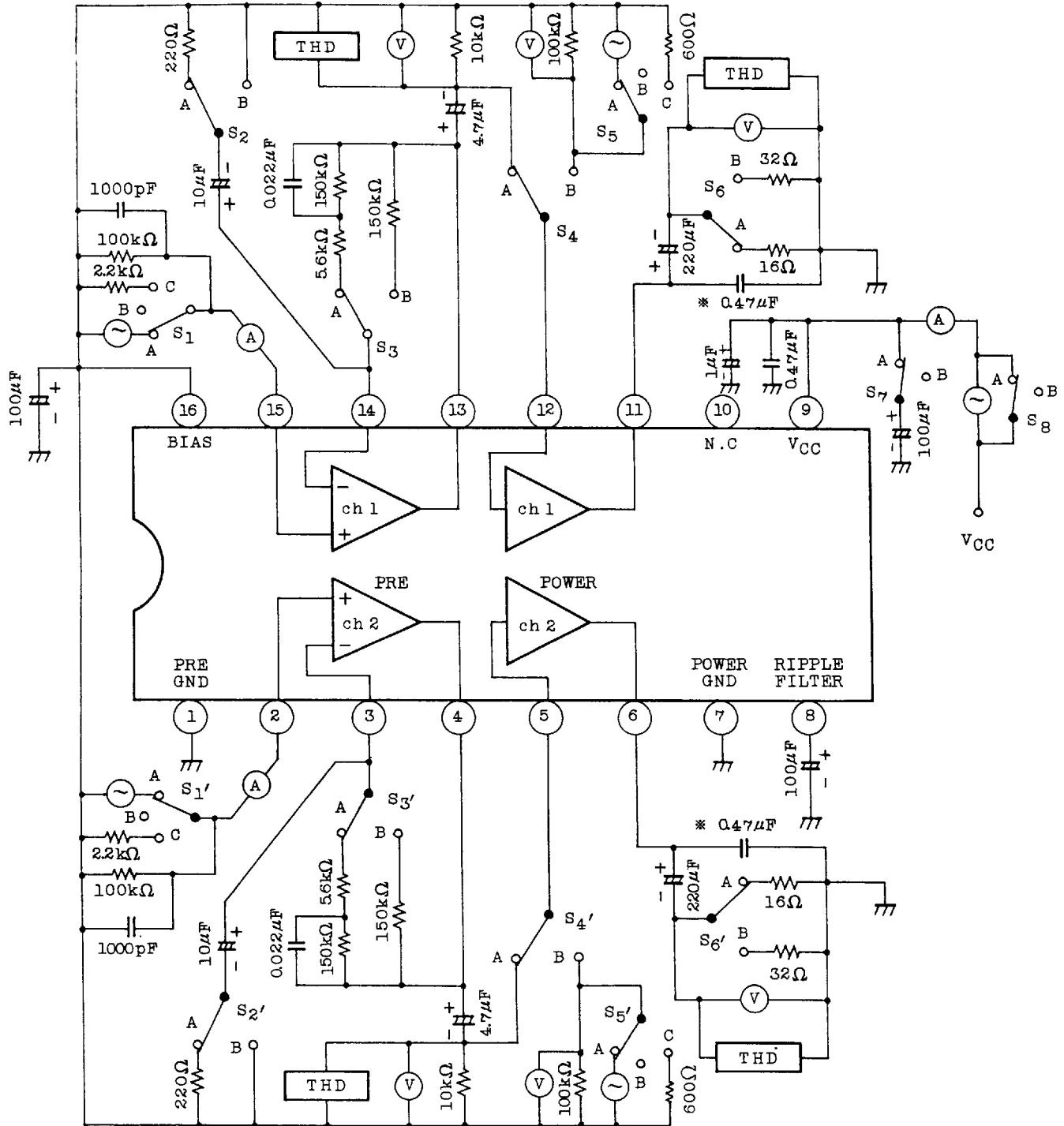
(PRE AMPLIFIER + POWER AMPLIFIER SECTION)

Channel Crosstalk	C.T		$R_g(Pre)=2.2k\Omega$ BW=~20kHz $V_{OUT}=-5dBm$	36	46	-	dB
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DC CHARACTERISTICS (No signal, $V_{CC}=3V$, $T_a=25^\circ C$)

PIN No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Terminal Voltage (V)	0	1.5	1.5	1.5	1.5	1.5	0	2.6	3.0	N.C	1.5	1.5	1.5	1.5	1.5	1.5

TEST CIRCUIT



* : Monolithic ceramic condenser

■ 9097247 0020163 56T ■

TA8111AP-3
1991-9-18
TOSHIBA CORPORATION

TEST METHOD

SYMBOL	S1	S2	S3	S4	S5	S6	S7	S8
ICCQ	B	A	A	A	*	A	A	A

(Pre Amp.)

GVO	A	B	B	B	*	*	A	A
THD	A	A	A	B	*	*	A	A
VOM	A	A	A	B	*	*	A	A
VNI	B	A	A	B	*	*	A	A
R.R	B	A	A	B	*	*	B	B
IB	C	A	A	B	*	*	A	A

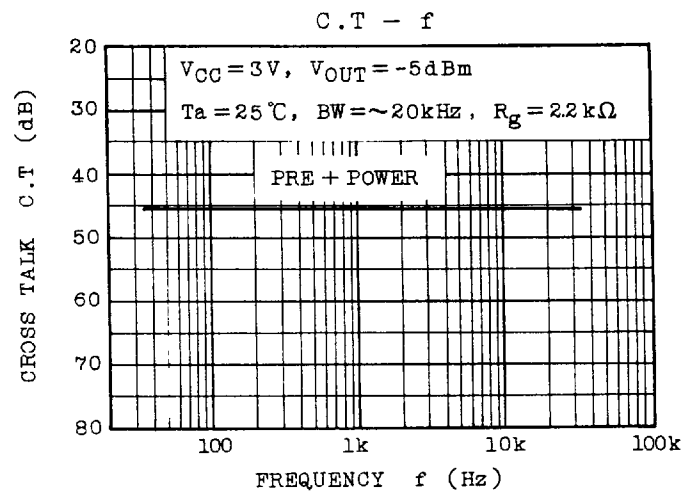
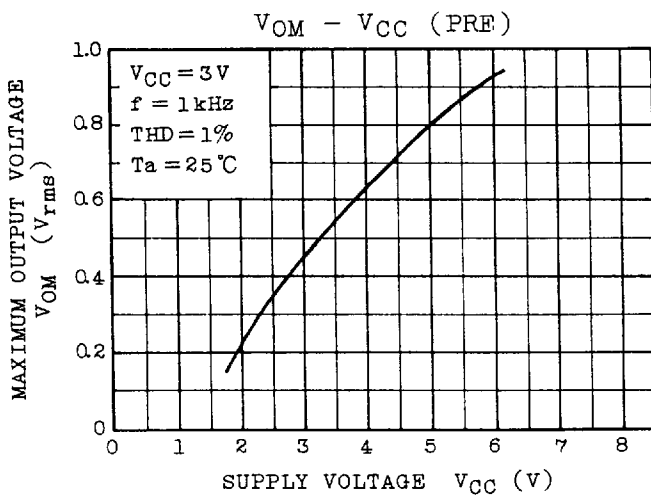
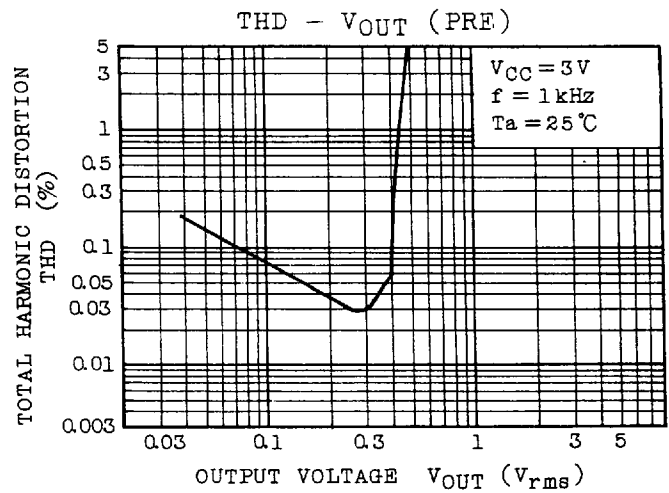
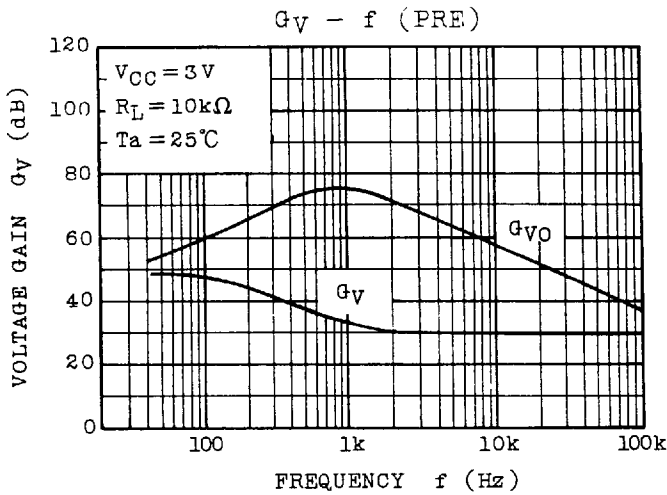
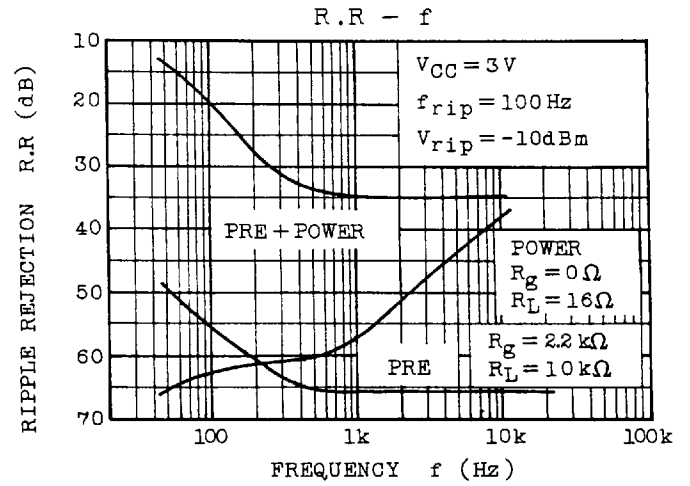
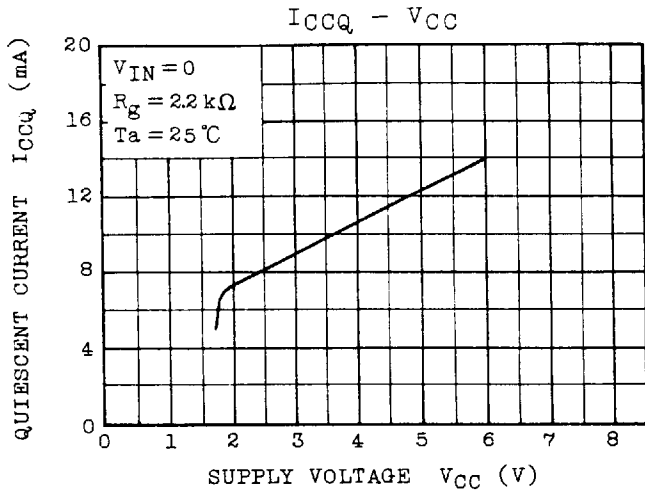
(Power Amp.)

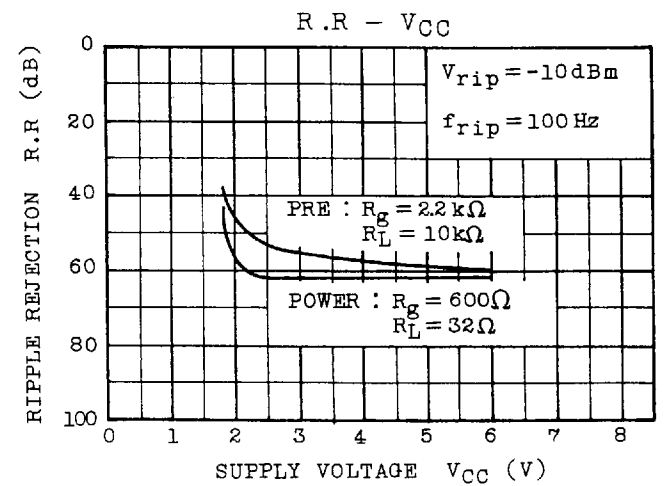
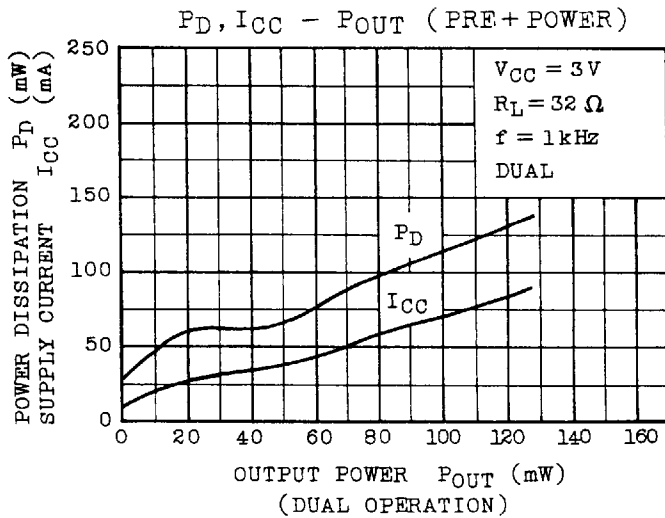
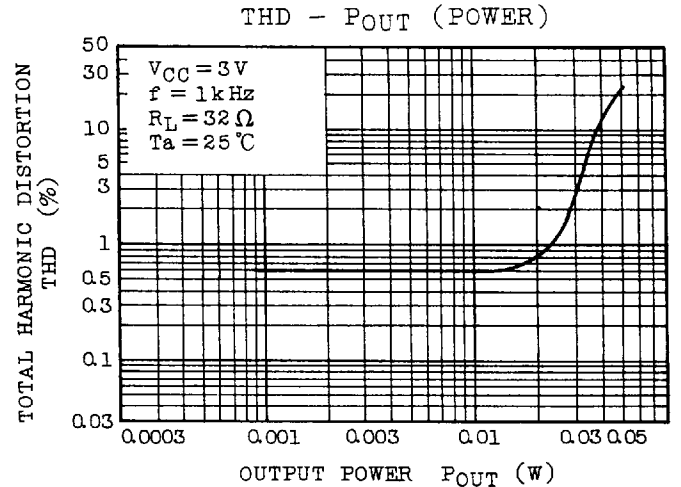
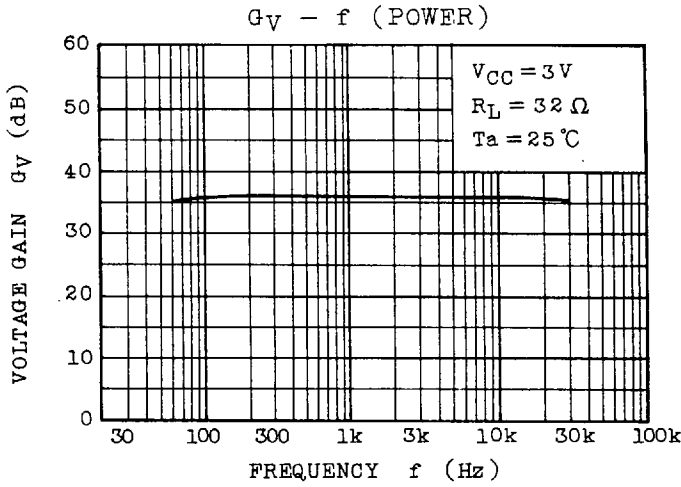
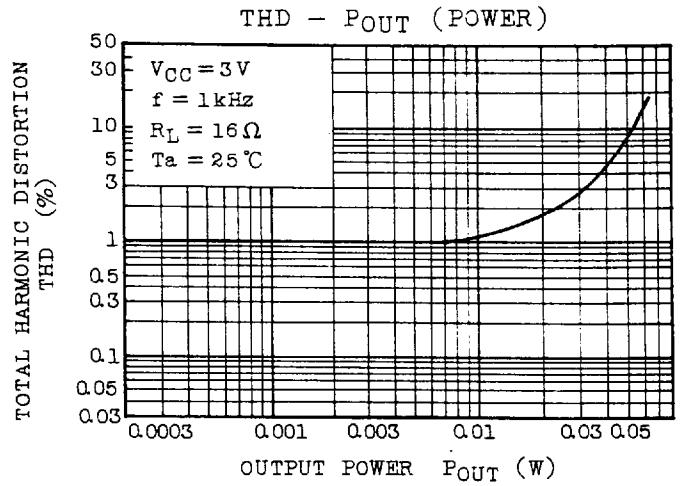
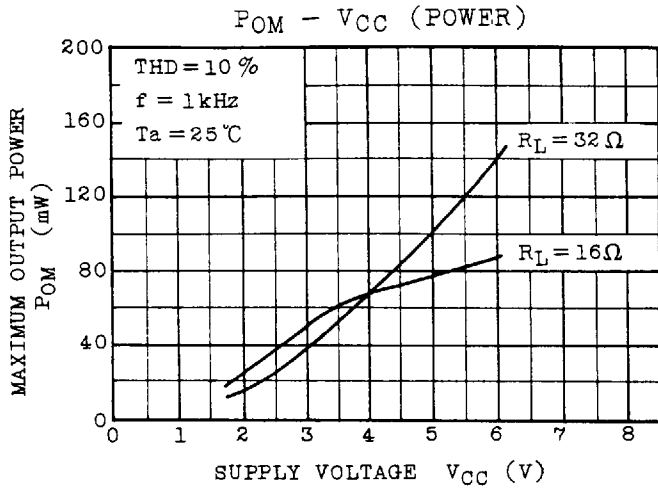
POUT1	*	*	*	B	A	A	A	A
POUT2	*	*	*	B	A	B	A	A
Gv	*	*	*	B	A	A	A	A
THD1	*	*	*	B	A	A	A	A
THD2	*	*	*	B	A	B	A	A
VNO	*	*	*	B	C	A	A	A
R.R	*	*	*	B	C	A	B	B
IB	*	*	*	B	B	A	A	A

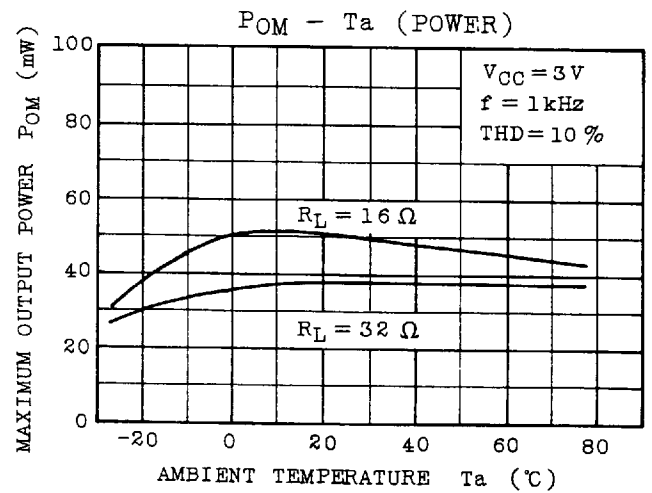
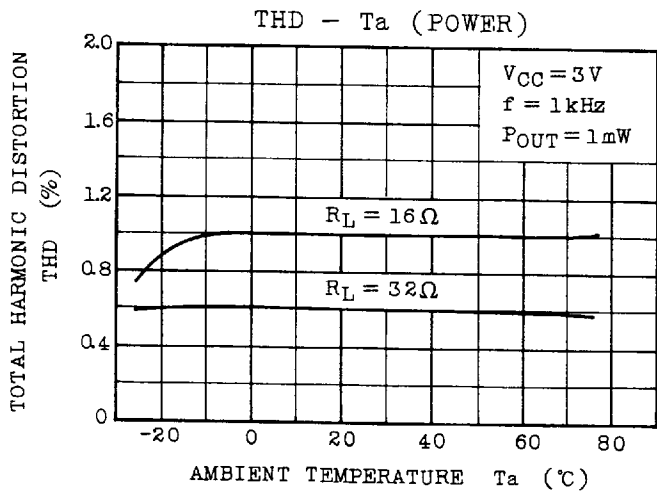
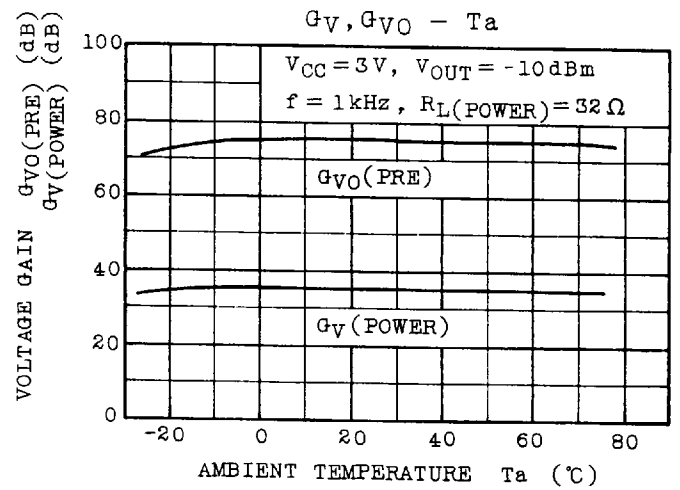
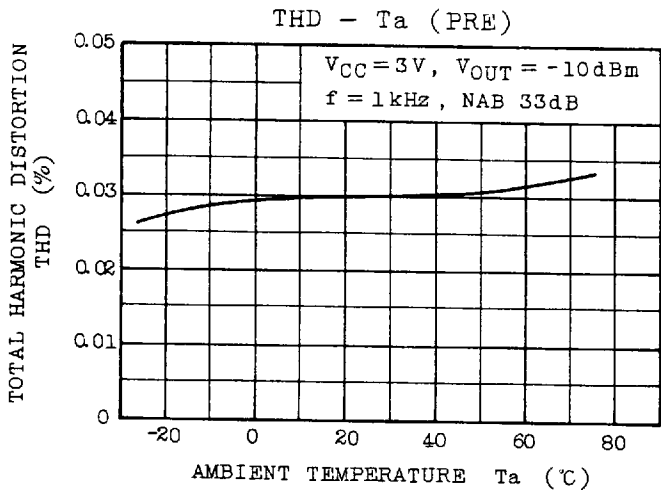
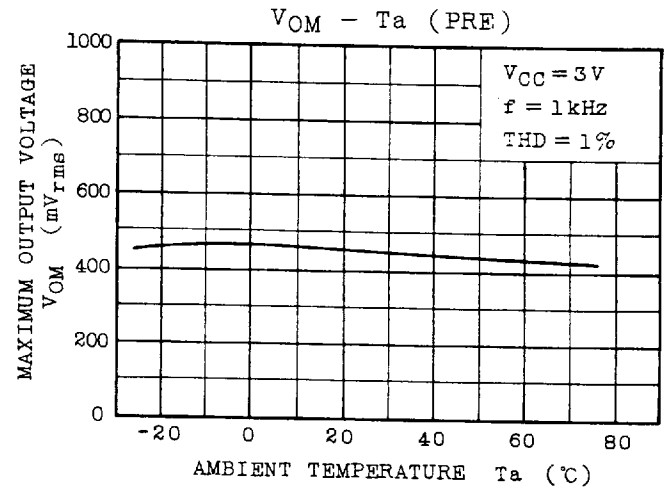
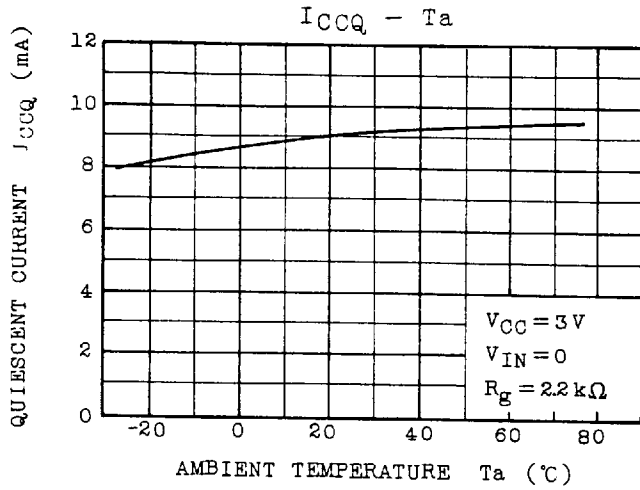
(Pre + Power)

C.T	A/B	A	A	A	*	A	A	A
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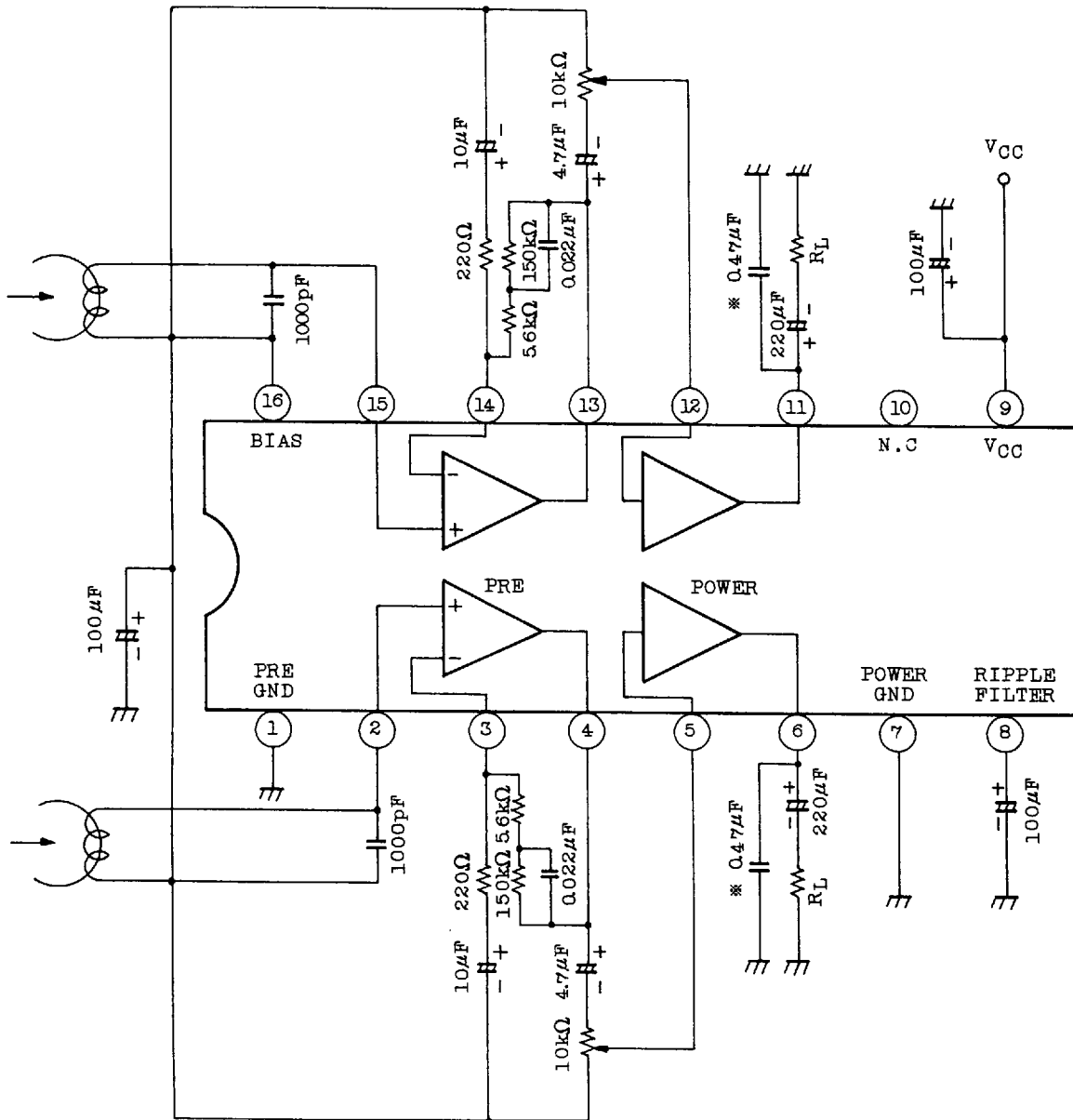
* No specified.





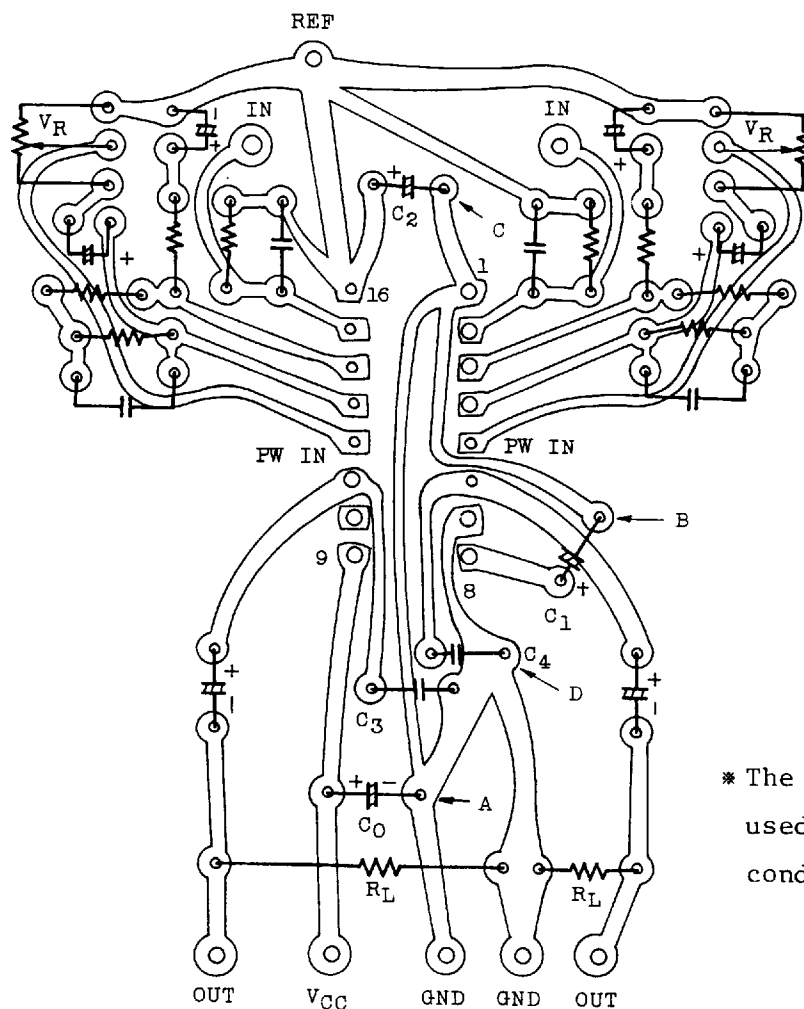


AN EXAMPLE FOR APPLICATION CIRCUIT



*: Monolithic ceramic condenser

AN INSTANCE FOR RECOMMENDED PCB PATTERN LAYOUT



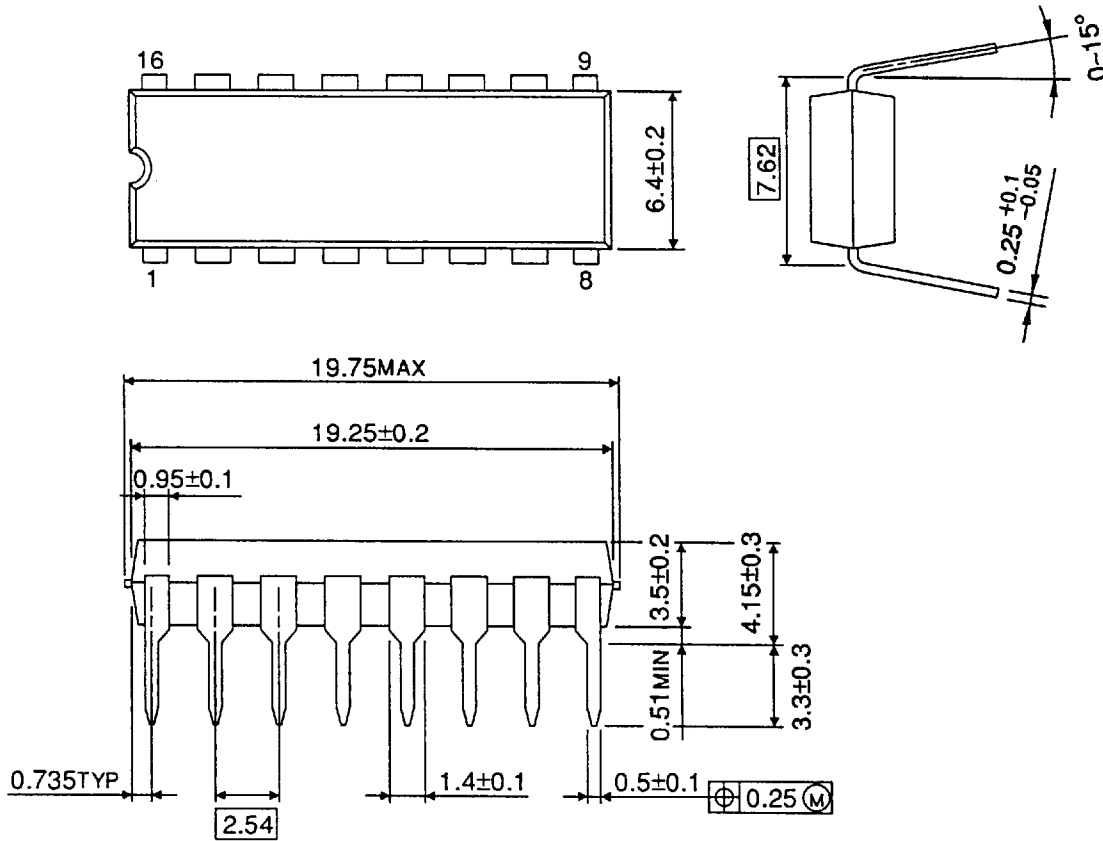
* The C3 and C4 must be used monolithic ceramic condenser.

REMARKS

- A : The 7 pin (power GND) and the 1 pin (pre.GND) must be isolated from GND(A) point of the V_{CC} coupling condenser (C₀).
- B : The GND point of the C₁ (B) and C₂ (C) must be connected to the 1 pin (pre. GND).
- C : The power input (5 pin and 12 pin) must be kept away from the power output (6 pin and 11 pin).
- D : The positive line of the C₃ and C₄ (output line) must be passed through inside of the IC pin form and the GND line of the those condensers must be connected to the 7 pin (power GND). It must be kept away as many as possible that the positive line of the C₃ and C₄ (output line) each other.
- E : The GND of the load must be connected to the D point where is the center line between the 7 pin (power GND) line to the GND line of the C₀.

OUTLINE DRAWING
 DIP16-P-300A

Unit in mm



Weight : 1.0g (Typ.)