Optimum power handling
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor
Type T171-250

Mean on-state current	I_{TAV}	250 A
Repetitive peak off-state voltage	V_{DRM}	300 ÷ 1800 V
Repetitive peak reverse voltage	V_{RRM}	
Turn-off time	t_q	80; 100; 160; 250 µs

V_{DRM}, V_{RRM}, V	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1800
Voltage code	3	4	5	6	7	8	9	10	11	12	13	14	15	16	18
T_j, °C	– 60 ÷ 125														

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	250	T_c=85 °C; 180° half-sine wave, 50 Hz	
I_{TRMS}	RMS on-state current	A	393	T_c=85 °C; Full cycle sine wave, 50 Hz	
I_{TSM}	Surge on-state current	kA	6.0 6.6	T_j=$T_{j\ max}$ T_j=25°C	180° half-sine wave, 50 Hz, single pulse; V_R=0 V; Gate pulse: 20 V, 5 Ω, 1 µs rise time, 500 µs
I^2t	Safety factor	$A^2s{\cdot}10^3$	180 218	T_j=$T_{j\ max}$ T_j=25°C	
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	300÷1800	T_j=$T_{j\ max}$; 180° half-sine wave, 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	335÷2000	T_j= $T_{j\ max}$; 180° half-sine wave, 50 Hz, single pulse Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75{\cdot}V_{DRM}$ $0.75{\cdot}V_{RRM}$	T_j=$T_{j\ max}$; Gate open	
TRIGGERING					
P_{GM}	Peak gate power dissipation	W	40	T_j=$T_{j\ max}$	
$P_{G(AV)}$	Mean gate power dissipation	W	6	T_j=$T_{j\ max}$	
V_{RGM}	Peak gate reverse voltage	V	5	T_j=$T_{j\ max}$	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current: non-repetitive repetitive	A/µs	 125 60	T_j=$T_{j\ max}$; V_D=$0.67{\cdot}V_{DRM}$; I_{TM}≤$2I_{T(AV)}$; Gate pulse: 20 V, 5 Ω, 1 µs rise time, 50 µs	
THERMAL					
T_{stg}	Storage temperature	°C	– 60 ÷ 50		
T_j	Junction temperature	°C	– 60 ÷ 125		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage	V	1.75	T_j=25°C; I_{TM}=3.14·I_{TAV}
$V_{T(TO)}$	On-state threshold voltage	V	1.00	T_j=$T_{j\ max}$
r_T	On-state slope resistance	mΩ	0.95	T_j=$T_{j\ max}$
I_L	Latching current	mA	700	T_j=25°C; V_D=12 V; Gate pulse: 20 V, 5 Ω, 1 µs rise time, 50 µs
I_H	Holding current	mA	250	T_j=25°C; V_D=12 V; Gate open
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and repetitive peak reverse currents	mA	30	T_j=$T_{j\ max}$; V_D=V_{DRM}; V_R=V_{RRM}
$(dV_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)]	V/µs	20 1000	T_j=$T_{j\ max}$; V_D=0.67·V_{DRM}; Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage	V	3.50	T_j=25°C; V_D=12 V; Direct gate current
I_{GT}	Gate trigger direct current	A	0.20	
V_{GD}	Gate non-trigger direct voltage	V	0.45	T_j=$T_{j\ max}$; V_D=0.67·V_{DRM}; Direct gate current
I_{GD}	Gate non-trigger direct current	mA	5.0	
SWITCHING				
t_{gt}	Turn-on time	µs	8.0	T_j=25°C; V_D=100 V; I_{TM}=I_{TAV}; Gate pulse: 20 V, 5 Ω, 1 µs rise time, 50 µs
t_{gd}	Delay time	µs		
t_q	Turn-off time[2)]	µs	80 100 160 250	T_j=$T_{j\ max}$; I_{TM}=I_{TAV}; di_R/dt=5 A/µs; V_R=100 V; V_D=0.67 V_{DRM}; dV_D/dt=50 V/µs
Q_{rr}	Recovered charge	µC	450	T_j=$T_{j\ max}$; I_{TM}=I_{TAV}; di_R/dt=5 A/µs; V_R=100 V;
t_{rr}	Reverse recovery time	µs	17.0	
THERMAL				
R_{thjc}	Thermal resistance junction to case	°C/W	0.15	Direct current, double side cooled

Note:

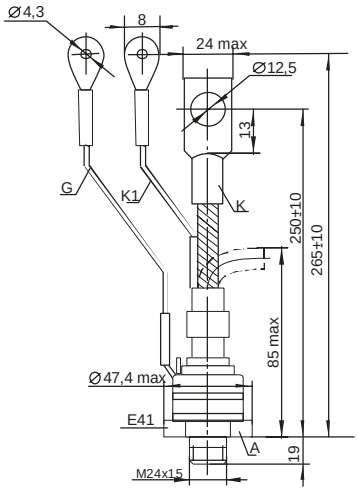
[1)] Critical rate of rise of off-state voltage

Symbol of group	P3	E3	A3	P2	K2	E2	A2
$(dV_D/dt)_{crit}$, V/µs	20	50	100	200	320	500	1000

[2)] Turn-off time

Symbol of group	B3	A3	T2	M2
t_q, µs	80	100	160	250

OVERALL DIMENSIONS



Weight: 440 grams
Tightening torque: 25 ÷ 35 Nm
Recommended heatsink: O181; O281

PART NUMBERING GUIDE

T	171	250	18	A2	B3	N
1	2	3	4	5	6	7

1. Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time
7. Ambient conditions: N – normal; T – tropical

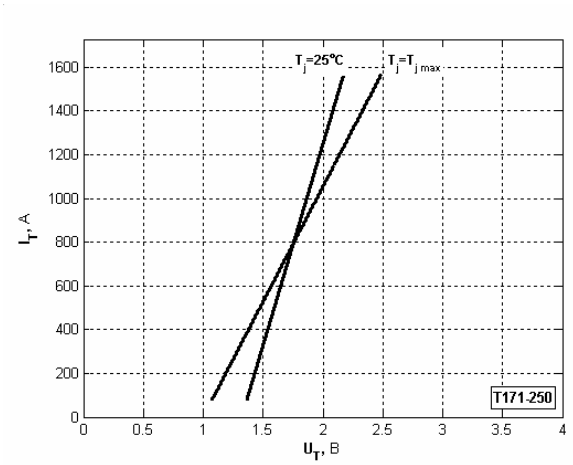


Fig 1 On-state characteristics

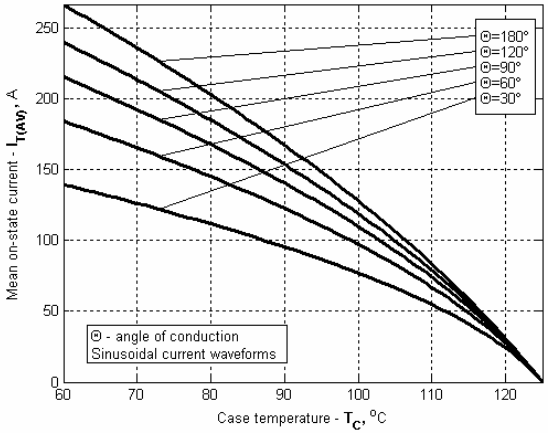


Fig 2 Maximum allowable mean on-state current I_{TAV} vs. case temperature T_C for sinusoidal current waveforms, f=50 Hz

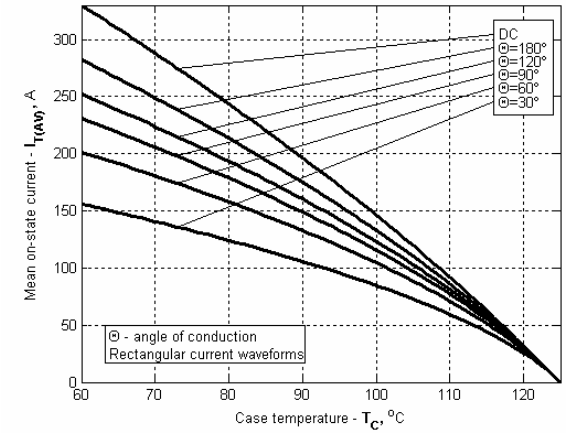


Fig 3 Maximum allowable mean on-state current I_{TAV} vs. case temperature T_C for rectangular current waveforms and for DC, f=50Hz

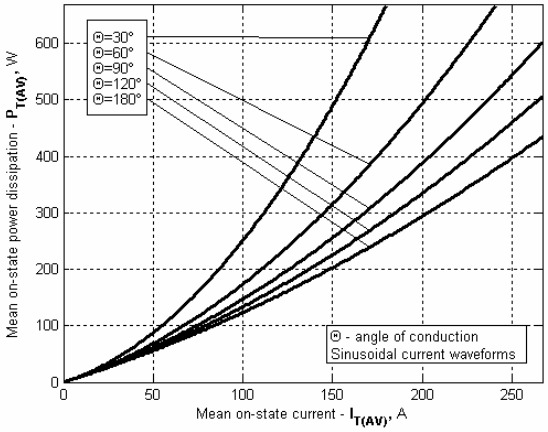


Fig 4 On-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles,f=50Hz

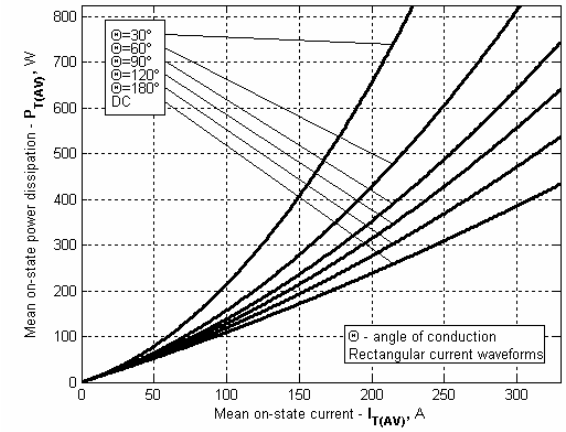


Fig 5 On-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms and for DC at different conduction angles, f=50Hz

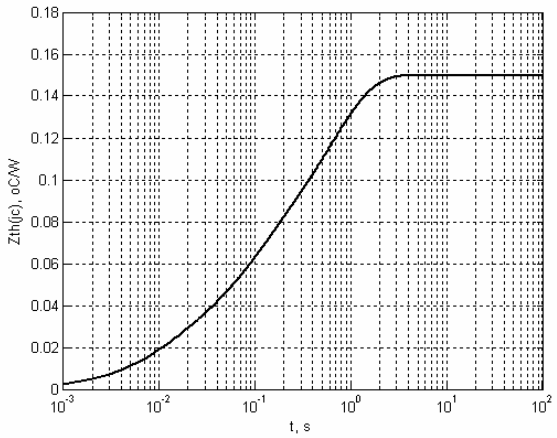
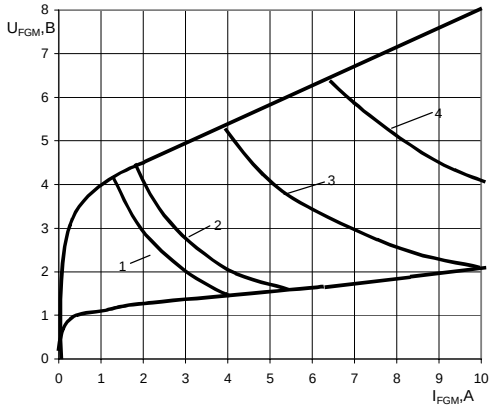


Fig 6 Transient thermal impedance junction to case $Z_{th(jc)}$



Position (See Fig. 7)	On-Off time ratio	Gate pulse length, ms	Gate Pulse Power, W
1	1	DC	6
2	2	10	8
3	20	1	20
4	40	0,5	40

Fig 7 Max. peak gate power loss: